10-BIT, 1GS/S TIME-INTERLEAVED SAR ADC

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ABSTRACT

This paper describes the implementation of a 4-channel, 10-bit, 1 GS/s time-interleaved analog to digital converter (TI-ADC) in 65nm CMOS technology. Each channel consists of interleaved T/H and ADC array operating at 250 MS/s, with each ADC array containing 14 time-interleaved sub-ADCs. This configuration provides high sampling rate even though each sub-ADC works at a moderate sampling rate. We have selected 10-bit successive approximation ADC (SAR ADC) as a sub-ADC, since this architecture is most suitable for low power and medium resolution. SAR ADC works on binary search algorithm, since it resolves 1-bit at a time. The target sampling rate was 20 MS/s in this design, however the sampling rate achieved is 15 MS/s. As a result, the 10-bit SAR ADC operates at 15 MS/s with power consumption of 560 μW at 1.2 V supply and achieves SNDR of 57 dB (i.e. ENOB 9.2 bits) near nyquist rate input. The resulting Figure of Merit (FoM) is 63.5 fJ/step. The achieved DNL and INL is +0.85\-0.9 LSB and +1\-1.1 LSB respectively. The 10-bit SAR ADC occupies an active area of 300 μm × 440 μm. The functionality of single channel TI-SAR ADC has been verified by simulation with input signal frequency of 33.2 MHz and clock frequency of 250 MHz. The desired SNDR of 59.3 dB has been achieved with power consumption of 11.6 mW. This results in a FoM value of 60 fJ/step.

KEYWORDS

ADC, SAR, TI-ADC, LSB, MSB, T/H, SCDAC, CDAC, SFDR, SINAD, SNR, TG, EOC, D-FF, MIM, MOM, DNL, INL.

1. INTRODUCTION

Time-interleaved analog to digital converters (TI-ADC) use a parallel combination of multiple sub-ADCs into a single ADC, that can improve the sampling rate compared to the sub-ADCs alone. The major advantage of time-interleaved ADC is that it can improve the sampling rate in a given technology. In wide band applications like wireless communication, serial data links require A/D converters with high sampling rate to meet the channel bandwidth and power requirements. Existing high-speed ADCs require high power to meet the required sampling rate. However, many applications demand for high sampling rates while keeping the power consumption relatively low. In these cases, low powered sub-ADCs operating at lower sampling rates can be used with interleaving to achieve the required sampling rate. In the proposed design we have selected SAR ADC architecture for sub-ADCs, since this architecture is most suitable for low power and moderate sampling rate. The major design challenge for time-interleaved ADCs is matching the performance of the sub-ADCs used with respect to bandwidth, timing, offset and gain. Mismatch in the performance of sub-ADCs degrades its major specifications like SFDR, SNDR etc. required for wireless communications. The mismatch in sub-ADCs can be

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detected and corrected by using calibration methods either in analog or digital domain. This correction can remove the problems due to mismatch to a certain extent [6] [8]. The proposed design adds redundant sub-ADCs in each ADC array (each channel) to enable background calibration. This paper describes the design procedure for a 10-bit 1 GS/s TI-ADC and implementation of a 10-bit SAR ADC. The TI-ADCs consist of a total of 4 × 14 i.e. 56 time-interleaved SAR ADCs, with each SAR ADC working at 20 MS/s (250M/13 ~ 20 MS/s) sampling rate to meet the overall sampling rate of 1 GS/s. Each SAR ADC consists of comparator, DAC and SAR logic. The rest of the paper is organized as follows: Section-2 describes the 4-Channel TI-ADC Architecture. Section-3 describes the Implementation of 10-bit 20 MS/s SAR ADC. Section-4 provides layout design and post layout simulation results. Section-5 describes the implementation of single channel TI-SAR ADC. Finally, the conclusions and future work are given in Section-5.

2. 4-CHANNEL TI-ADC ARCHITECTURE

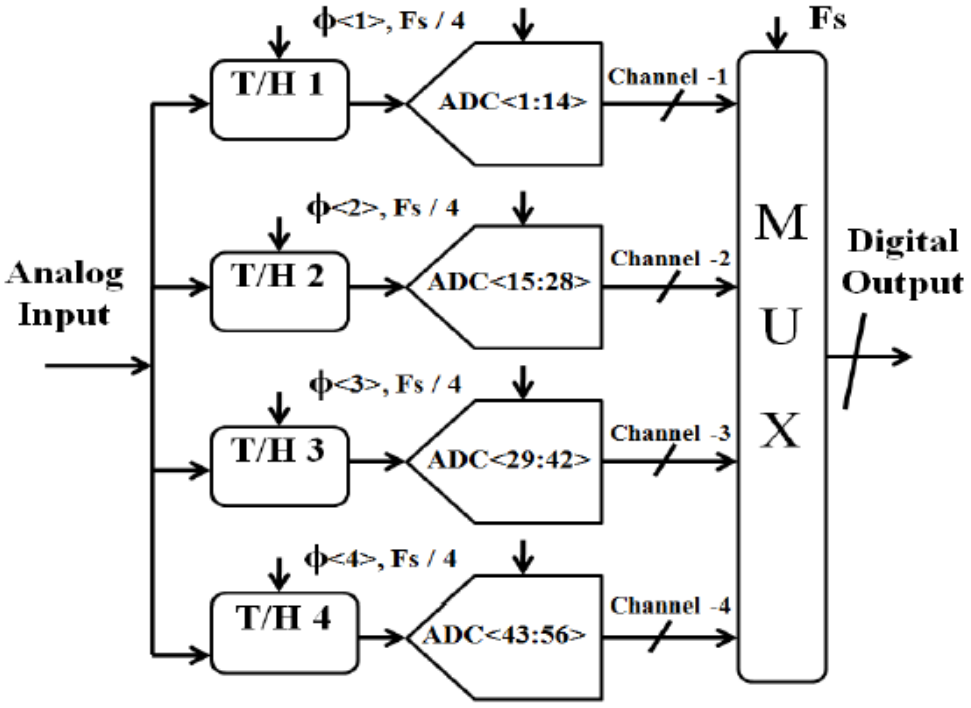

Figure 1. Architecture of 4-Channel TI-ADC.

Fig. 1 shows the architecture of the 4-channel TI-ADC, each channel consists of time-interleaved T/H and ADC array, each ADC array uses 14 time-interleaved 10-bit SAR ADCs. The 4-channels are driven by clock frequency of Fs/4, with equally spaced phases, $\phi< 1 >$ to $\phi< 4 >$. In a TI-ADC with sampling rate (Fs) of 1 GS/s, each channel should operate at Fs/4 = 250 MS/s with equally spaced phases at $\phi < i > = 2\pi (i - 1)/4$ where i = 1, 2, 3 etc. (0º, 90 º, 180 º, 270 º). Sampling rate of each SAR ADC should be 20 MS/s. The additional 10-bit SAR ADC used in each channel is for background calibration. Fig. 2 shows the timing diagram of 4-channel TI-ADC at each rising edge of master clock (Fs). The track and hold unit of each channel spends two clock cycles in track mode and two clock cycles in hold mode. This choice of timing presents a trade-off between input bandwidth and accurate sampling of the input. Since the operation of each channel is shifted with respect to the previous one by one clock cycle, at any given time,

only two channels are in track mode. This implies that at any moment of time N=2 ('N' represents number of channels) sampling capacitors are connected to the input. While this limits the bandwidth [5], it gives enough settling time for sampling the data (two clock cycles) to the T/H unit. When the first T/H goes from track mode to hold mode it has acquired a sample of the analog input over two clock periods.

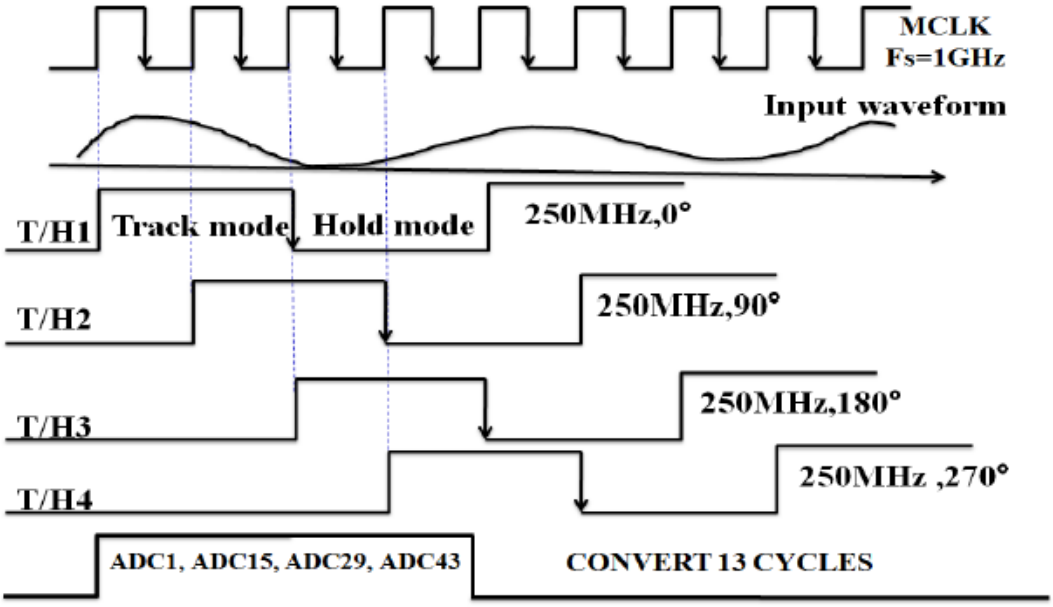

Figure 2. Timing diagram of 4-channel TI-ADC.

It is then converted to digital domain by the corresponding sub-ADCs in each channel. The master clock (Fs) works at 1 GHz while each track/hold and sub-ADC works at 250 MHz clock frequency with appropriate phase shift.

2.1. Limitations of Time-Interleaved ADC

The optimum number of channels are chosen based on the required sampling rate. To achieve high sampling rate, increasing the number of channels is not desirable because of offset, bandwidth, timing and gain error mismatches between the channels. Mismatch in the channels degrades the performance of time-interleaved ADC. Corrections for these mismatches can be implemented to a certain extent using calibration in either digital or analog domain. However, the calibration process in time-interleaved ADCs is constrained by the number of channels.

3. IMPLEMENTATION OF 20MS/S 10-BIT SAR ADC

A Successive approximation register (SAR) ADC works on binary search algorithm principle. Fig. 3 shows the block diagram of fully differential 10-bit SAR ADC. It consists of comparator, capacitive DAC (CDAC) & SAR logic. Binary search algorithm proceeds along the following steps to convert the analog input into its equivalent digital output [13]. The first step is to sample the differential inputs during sampling phase using CDAC. Next step is to set the 10-bit register in SAR logic to mid code (i.e., 1000...00, here MSB is '1'), this forces the 10-bit CDAC to V_{pref} /2 where V_{pref} is positive reference voltage to the CDAC. The comparator compares the

differential DAC outputs (i.e., V_p = - V_{inp} + V_{pref} /2 & V_n = -V_{inn}+V_{pref} /2). If the V_n > V_p (i.e., V_{inp} > V_{inn}) then MSB will remain at active high otherwise it will be forced to active low. After resolving MSB bit, the SAR logic moves to next bit, it forces that bit active high and does another comparison, this process is repeated for 10-bits till it reaches to least significant bit (LSB). Then 10-bit digital output code is available at end of conversion (EOC).

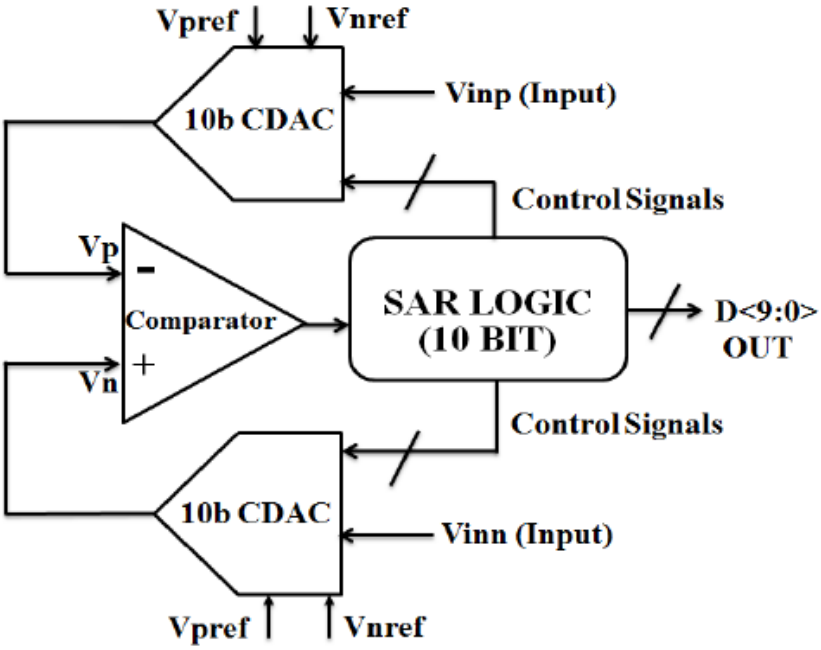

Figure 3. Block diagram of 10-bit SAR ADC

Since, SAR ADC resolve the input one bit at a time, the complexity and power consumption is lower at expense of reduced sampling rate. 10-bit SAR ADC requires the 10 + 3 clock cycles to get the digital output for given analog input inclusive of two cycles for sampling the input with comparator offset calibration before the conversion takes place and another cycle for data latch after the conversion. This cycle signal is called end of conversion (EOC).

3.1. 10-bit Fully Differential Capacitive DAC

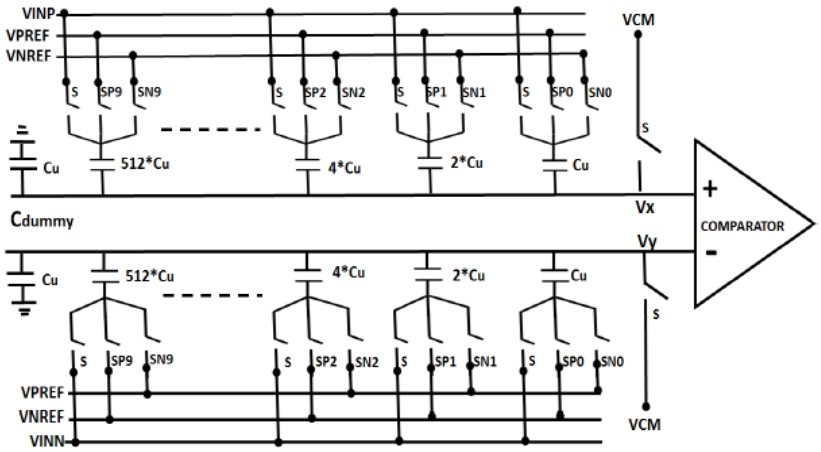

Figure 4. Architecture 10-bit fully differential CDAC

Fig. 4 shows architecture of 10-bit fully differential capacitive DAC (CDAC). It performs both sampling (S/H) operation as well as DAC operation. CDAC switching mechanism is controlled with SAR logic based on the comparator decision. In 10-bit CDAC, the capacitor network is in binary weighted fashion with dummy capacitor, Where C_u is a unit capacitor. For simplicity, the explanation given here is for a single sided CDAC. The same is applicable for a fully differential CDAC. During the sampling phase (S), the top plates of the capacitors in network are connected to common mode voltage (V_{cm} = 0.6 V) through a switch and bottom plates are charged to the input voltage (V_{inp}). The total charge on the capacitor during sampling phase is calculated by $Q_{tot} = 2^n * C_u (V_{cm} - V_{inp})$ for an n-bit CDAC. During the next cycle, the top plate switch is opened before the SAR logic sets the MSB bit to high ('1') thus the bottom plate of the MSB capacitor is now connected to V_{pref} (1.2 V). The remaining capacitors are connected to V_{nref} (0 V). Since the top plate is connected to a high input impedance of the comparator, the total charge on capacitors remains the same [14]. However, switching causes the charge to redistribute resulting in the top plate potential going to V_x. The total charge on top plate capacitor is given by

$$Q_{tot} = Q_{MSB} + ... + Q_{LSB} + Q_{dummy} \quad (1)$$

$$2^n C_u (V_{cm} - V_{inp}) = 2^{n-1} C_u (V_x - V_{pref}) + 2^{n-1} C_u (V_x) \quad (2)$$

$$V_x = - V_{inp} + V_{cm} + V_{pref} /2 \quad (3)$$

If $V_x < V_{cm}$, it means $V_{inp} > V_{pref} / 2$ and the most significant bit (MSB) value is set to high, otherwise it is reset to low ('0'). In next cycle the second MSB bit is set to high, which results in a comparison with either $3V_{pref} /4$ or $V_{pref} /4$, depending on the value of MSB bit, this process continues till the CDAC converges to V_{cm} (common mode voltage) and the LSB is determined. The major advantage of capacitive DAC is that it is less sensitive to parasitic effects across the capacitor array, which improves linearity (monotonic) at the DAC outputs.

3.2. Selection of Unit Capacitor (C_u) and Switch

The value and type of unit capacitor is chosen based on area and mismatch data given in UMC65nm CMOS technology. This technology has two different types of capacitors (i) MOM

Capacitor (ii) MIM Capacitor. MIM capacitor is more accurate compared to MOM capacitor, but it occupies more area. The value of unit capacitor is limited by thermal and quantization noise (i.e., the sum of rms thermal noise and rms quantization noise to be less than LSB/2). $KT/C_{total} + LSB^2/12 < (LSB/2)^2$, where $LSB = 1.2/2^{10} = 1.17$ mV, therefore C_{total} should be greater than 100 fF. Also, the total capacitance for 10-bit CDAC is $2^{10} * C_u = C_{total}$, where C_u unit capacitance. This gives a unit capacitance of $C_u > 100$ aF [15]. Choosing a lower value capacitance reduces the switching power and area but mismatch between capacitor arrays become very high which leads to non-linearity. In this design considering the area constraint, switching power and mismatch factors, the chosen unit capacitance (C_u) value is 10 fF which occupies an area of 4 µm * 4 µm. Transmission gates (TG) were used as switches to meet the settling error within LSB/2, given the settling time (800 pS) during the sampling phase. Considering the unit capacitance of 10 fF, the total capacitance during the sampling phase, $C_{hold}=2^{10} * 10$ fF =10.24 pF. The settling time of DAC output is 4 ns ($5* R_{on} * C_{hold} = 4$ ns) with clock frequency of 250 MHz) so, the ON-resistance of switch should be less than 78 Ω (i.e., Ron <78 Ω). Which leads to TG transistor (Both NMOS and PMOS) sized with W = 10 µm and L = 0.1 µm.

3.3. Selection of Comparator Architecture

The comparator is a key component in an analog to digital converter (ADC). Every ADC contains at least one comparator (1-bit A/D converter). It must be able to resolve very small analog voltage and convert it into a rail-to-rail digital output. This small input voltage is known as the resolution of the comparator. The basic function of the comparator is to compare the differential input signal with the reference threshold and to give a digital decision accordingly. The architecture of the comparator is chosen based on resolution, speed, offset voltage and power dissipation. A dynamic latch comparator is most widely used for high speed and low power consumption. The main disadvantage of latch type comparators is their high input offset voltage due to mismatch in transistors and also the kick back noise effect at the inputs. To reduce the input offset voltage and the effect of kick back noise, a preamplifier is used in front of the dynamic latch. The requirements from the comparator are:

- Resolution (LSB) = 1.17 mV
- Input offset voltage and input integrated noise < LSB/2
- Settling time < 800ps, considering 250 MHz as clock frequency

3.4. Architecture of Preamplifier Based Dynamic Latch Comparator

Fig. 5 shows the schematic of preamplifier based dynamic latch comparator. It consists of three stages viz preamplifier, dynamic latch and SR latch. Preamplifier is a differential amplifier with resistive load (R0, R1 = 5 KΩ) with wide bandwidth and relatively small gain to achieve high speed as shown in Fig. 5a. The dynamic latch consists of two cross-coupled CMOS inverters used for regeneration as shown in Fig. 5b. It operates in either one of the following two modes:

- Rest phase (CLK = LOW)
- Evaluation phase (CLK = HIGH)

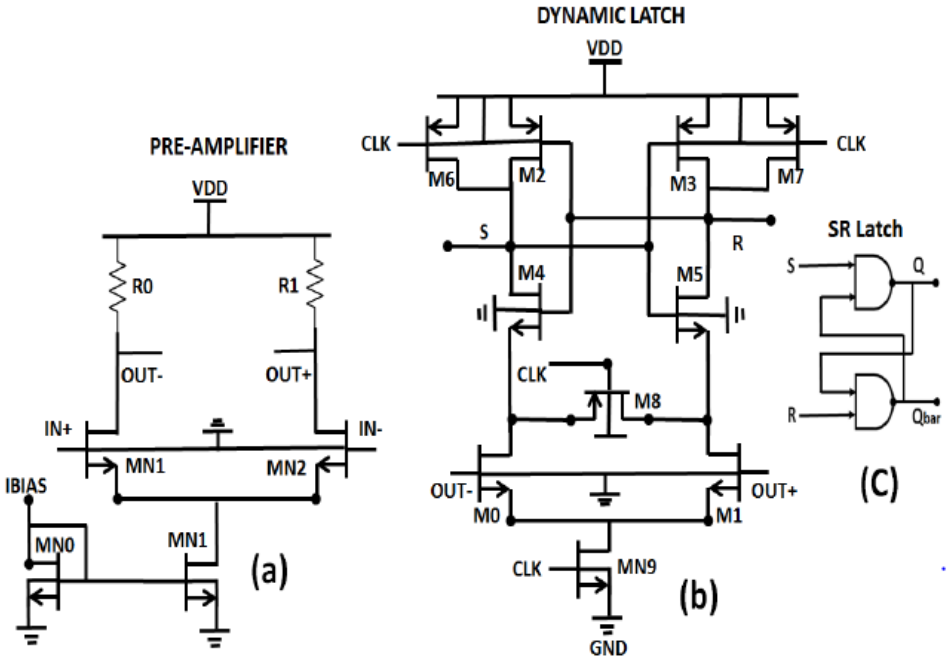

Figure 5. Schematic of preamplifier based dynamic latch

During the reset phase, the output nodes of cross coupled inverters (M2-M5) are reset to V_{DD} through the reset transistors M6 and M7. During the evaluation phase, the tail transistor MN9 is turned on. The input transistor pairs (M0, M1) start discharging at different time rates depending on the applied input voltage. This initiates positive feedback, enhancing the small differential voltage to a full swing differential output. The mismatch of transistor size in differential pair (M0, M1) and threshold voltage variation between M4, M5 transistor can lead to high input offset voltage. This offset voltage can be reduced by keeping a preamplifier in front of the dynamic latch which also prevents kick back noise to the differential inputs. The gain of the preamplifier is 19.5 dB with unity gain bandwidth (UGB) of 5 GHz, input offset voltage of ±872 µV and input integrated noise (100 Hz to 5 GHz) of 715 µV (rms).

3.5. 10-bit Successive Approximation Register Logic

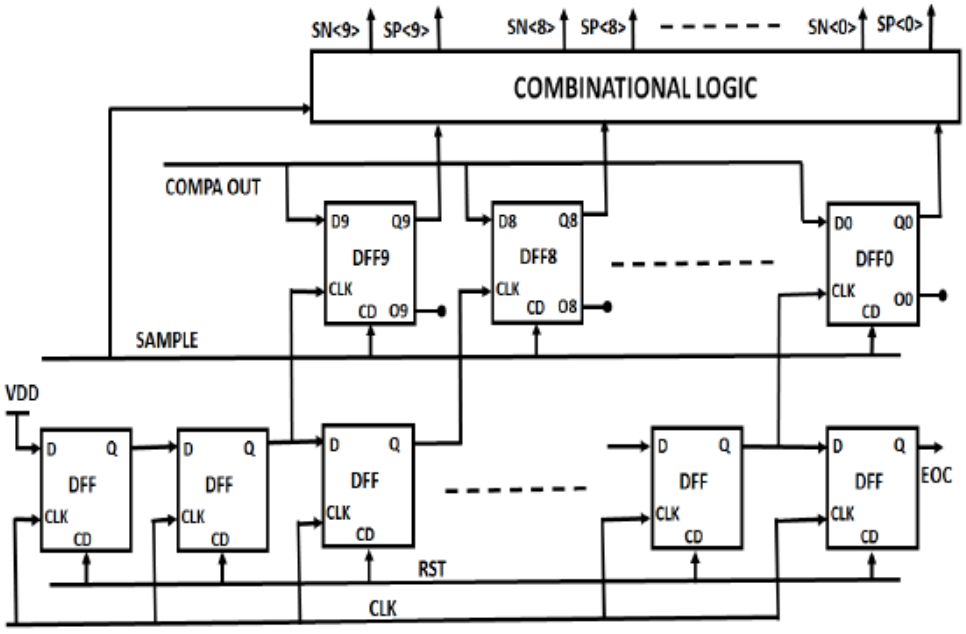

Figure 6. Block diagram of 10-bit SAR logic

There are two kinds of approaches to design SAR logic. One is a method proposed by Anderson [17] and the other is Rossi and Fucili method [18]. Fig. 6 shows 10-bit SAR logic proposed by Anderson. It is based on shift registers and combination logic. In this design, the binary search 10-bit SAR logic is implemented using this approach. The proposed 10-bit SAR logic requires at least 2*10 = 20 D-FFs. One chain of 10 D-FFs for storing the conversion results and another chain of 10 D-FFs for performing the shift operation and generation of necessary control signals (SN< 9:0 >, SP< 9:0 >) for DAC operation using combinational logic. SAR logic performs three main operations, (i) It shifts the initial mid code (i.e.,1000...00, here MSB is '1') to the right by one bit (ii) It loads the result from the comparator (COMPA OUT) during the positive edge triggering of next nearest bit (iii) Finally it holds the converted bits. After 10 clocks, shift registers generate pulse called end of conversion (EOC), which means that the whole conversion is completed. The EOC also indicate the start of the next sampling.

4. LAYOUT DESIGN & POST LAYOUT SIMULATION RESULTS

4.1. Transient response of 10-bit CDAC

Fig. 7 shows the transient response of differential CDAC (V_x, V_y nodes shown in Fig. 4) with DC input voltages V_{inp} = 1.1 V and V_{inn} = 0.1 V at 10 MS/s sampling rate. The corner (typ, min, and max) and monte-carlo simulations have been carried out for differential CDAC and the

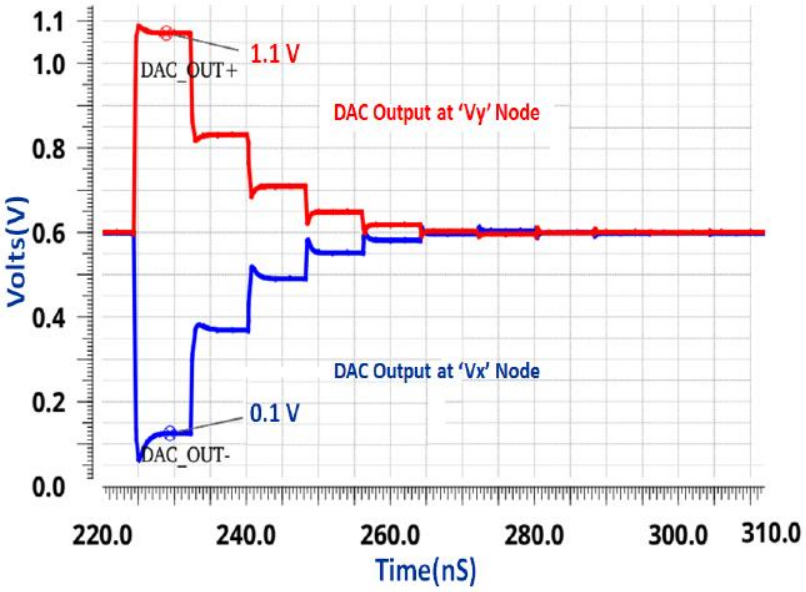

Figure 7. Transient response of 10-bit CDAC

output voltage variation of about ±900 µV at maximum input voltage (i.e., <LSB) is seen. DAC output voltages are settled within 0.5 LSB of the final value. The dynamic power (i.e., C_{total} * V_{DD}^2 * Fs) of 10-bit CDAC is 150µW with 1.2 V supply at 10 MS/s.

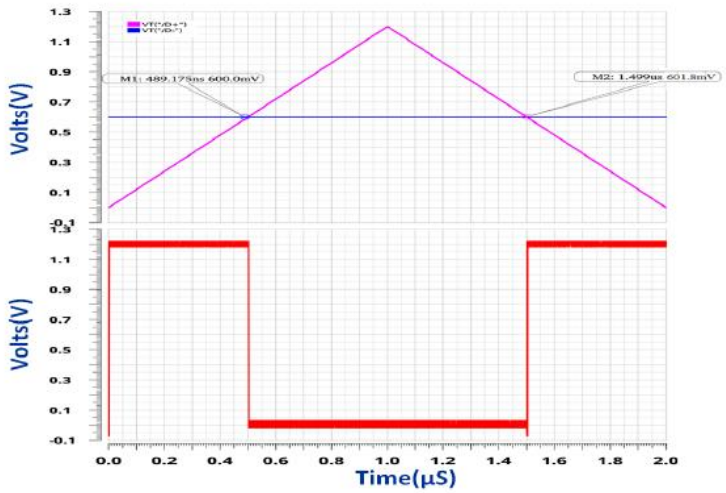

Figure 8. Transient response of dynamic comparator

Fig. 8 shows the transient response of comparator with triangular input signal and with a common mode voltage of 0.6 V. To estimate the input offset voltage of preamplifier-based latch comparator, Monte-Carlo simulations were carried out (number of runs = 50) and the comparator output transition were seen to be shifted towards positive and negative side in time which results an input offset voltage deviation of ±872 µV about the mean value respectively as shown in Fig. 9

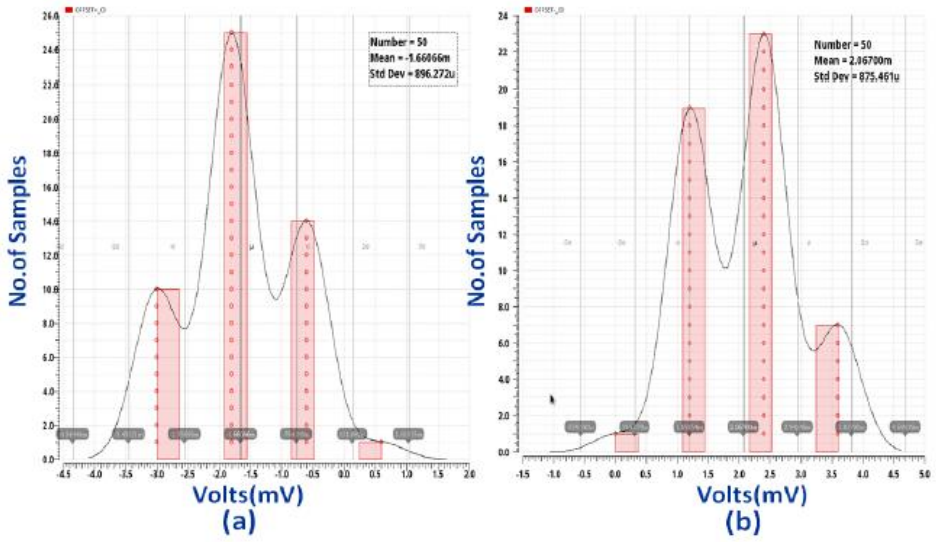

Figure 9. Preamplifier based dynamic latch comparator input offset voltage (a) at negative terminal (b) at positive terminal

4.2. Transient Response of 10-bit SAR Logic

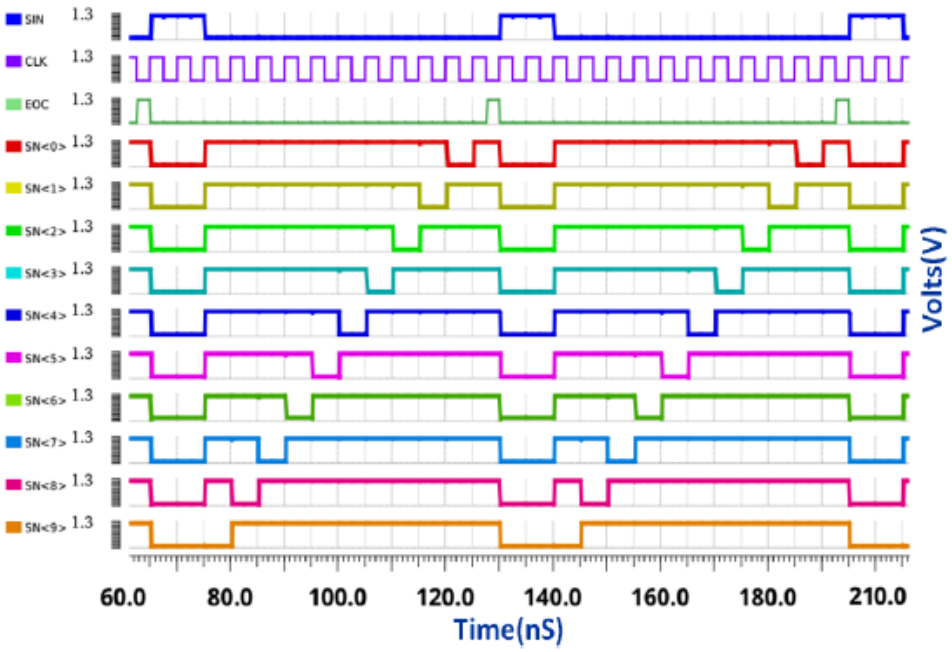

Figure 10. Transient response of 10-bit SAR logic

Fig. 10 shows the transient response of 10-bit SAR logic. The clock frequency of 250 MHz pulse input (period = 4 ns) is given to MOD-13 counter to generate the sample pulse (SIN). It repeats for every 13 cycles (i.e 13*4ns = 52 ns). 10-bit shift register used for generating the EOC pulse (T_{pulse} = 4 ns) just before the next sampling. The shift register and combination logic is used for generating control signals (SN< 0 >, SN<1 > .. SN< 9 > and SP< 0 >, SP< 1 > .. SP< 9 >) based on comparator decision (COMPA OUT).

4.2. Layout Design & Dynamic Performance of 10-bit SAR ADC

Fig. 11 shows the layout of 10-bit SAR ADC. In this design, the METAL stack with maximum metal width is used for routing critical nets like differential CDAC outputs, comparator output in a symmetric manner to avoid the output voltage mismatch, delay due to parasitic effects. All control signals which control the switching of CDAC are laid out symmetrically to meet the equal delay effect. The total area occupied by 10-bit SAR ADC is 300 µm * 440 µm.

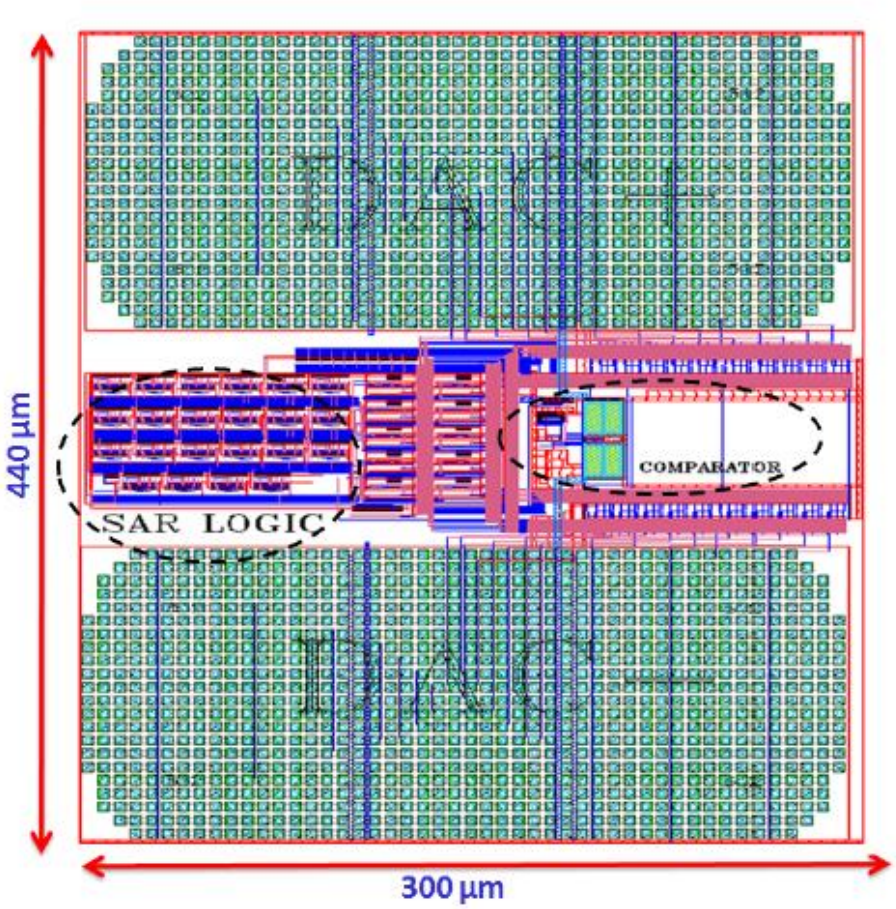

Figure 11. Layout of 10-bit SAR ADC

The coherent sampling method is used for evaluating dynamic performance of ADC as shown in Fig. 12b, the transient noise simulation is carried out to include quantization, thermal noise effects (F_{max} is chosen as maximum clock frequency given for ADC i.e., 250 MHz). The following inputs are given for evaluating the dynamic performance of 10-bit SAR ADC. V_{in} = 1 V_{p-p}, $F_{in} = F_s/2$ (i.e., nyquist rate input), F_s =15 MS/s and no. of points is 128. The achieved SFDR is 64.5 dB and SNDR of 57 dB (ENOB = 9.2 bits).

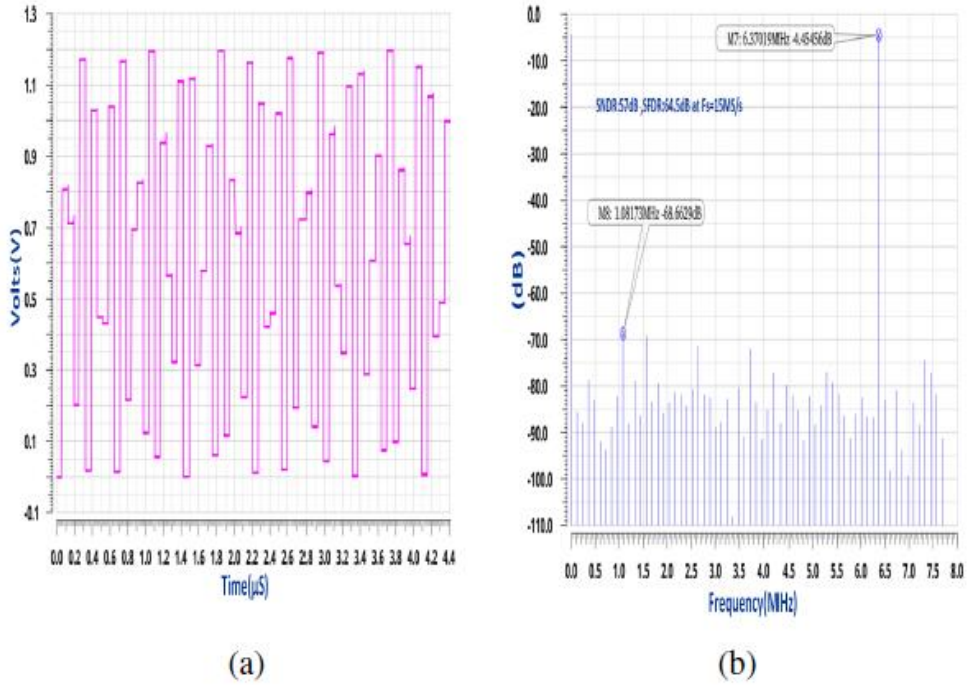

Figure 12. 10-bit SAR ADC (a) Transient response (b) Output Spectrum

4.3. Static Performance of 10-bit SAR ADC

The evaluation of static performance (DNL and INL) of 10-bit SAR ADC is done by using endpoint method with ramp input. The following inputs are given for evaluating the static performance of 10-bit SAR ADC, ADC sample rate is F_s=15 MS/s or T_s = 66 ns, resolution of ADC is 1.17 m V, for LSB/4 measurement the resolution per code becomes 4 samples/code and ramp duration per code will be 264 ns (i.e., 4*66ns). So, ramp slope is 1.17 mV/0.264 µs. The achieved DNL of +0.85 \ -0.9 LSB is shown in Fig. 13a and INL of +1.061 \ -1.124 LSB is shown in Fig. 13b. The major INL and DNL jump occurs at first and second MSB transition, which are due to capacitor mismatches [12].

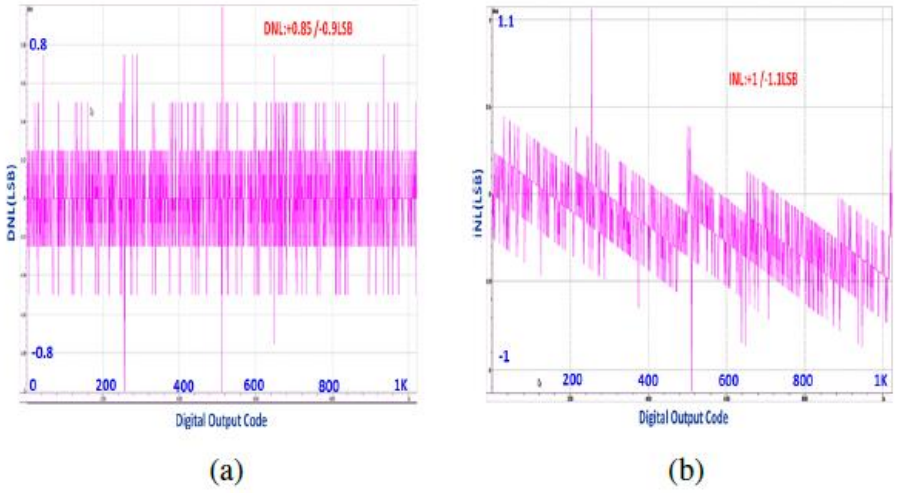

Figure 13: Static performance of 10-bit SAR ADC (a) DNL (b) INL

5. ARCHITECTURE OF SINGLE CHANNEL TI-SAR ADC

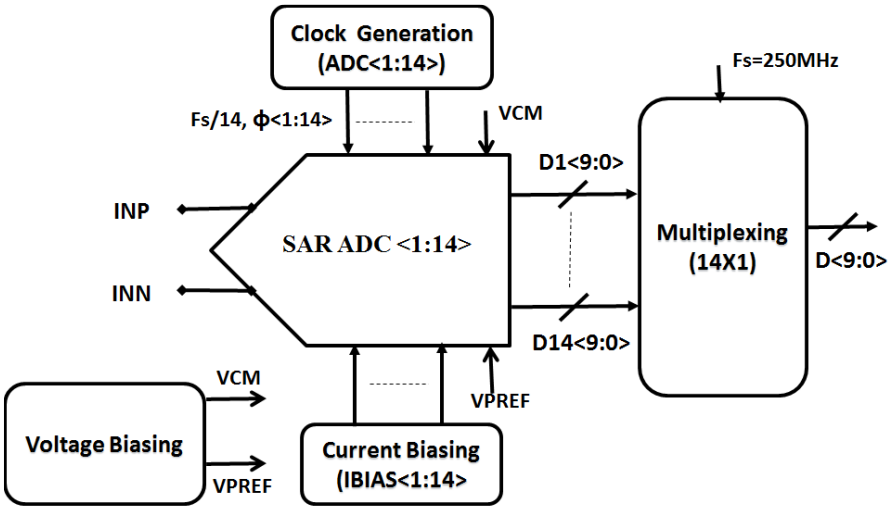

Figure 14. Block diagram of single channel 10 bit, TI-SAR

A Single Channel TI-SAR ADC architecture consist of the following sub-modules as shown in Fig. 14.

- Current Biasing
- Clock generation / Timing scheme
- Digital Multiplexing

5.1. Current Biasing

Fig. 15 shows the current basing circuit of single channel TI-SAR ADC. The two-stage differential amplifier (error amplifier) with gain of 65 dB is used to create the voltage controlled current source (voltage to current converter). In Fig. 15 shows the voltage to be converted is

applied to noninverting terminal of the amplifier. The inverting terminal of the amplifier is connected in negative feedback viz resistor and transistor MN0. The output of amplifier drives the input gate of the transistor MN0. The error amplifier will force the required gate voltage such that the voltage across resistor R0 need to be V_{ref} is equal to 0.6 V, which results the reference current in R0 and MN0 will be 120 µV (i.e., V_{ref} / R0). Further this reference current is pass through PMOS current mirror (M0 to M14) and mirror current is scaled down to 50 µA by sizing the PMOS transistor, finally the bias currents are (IBIAS< 1 > to IBIAS< 14 >) fed to comparators of 14 TI-SAR ADC.

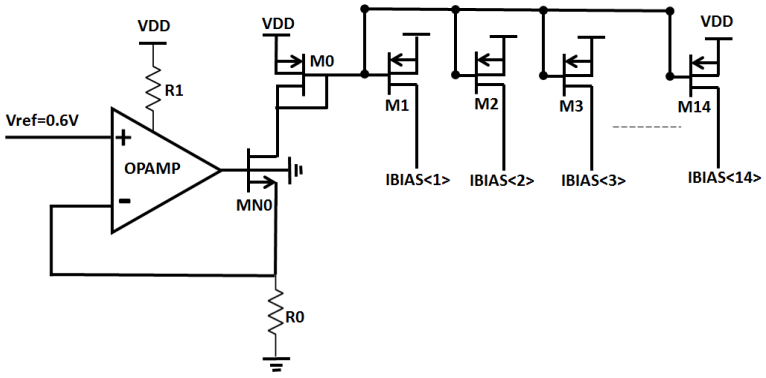

Figure 15. Schematic of voltage to current converter

5.2. Timing Scheme/Clock Generation

Fig. 16 shows the timing scheme of single channel time-interleaved SAR ADC. It is based on shift register. In this design, the timing signals (ADC< 1 > to ADC< 14 >) for operation of TI-SAR ADC are generated by cascading the DFFs, so that the output from the previous flip-flop becomes input to the next flip-flop. While performing shift operation the timing signals are shifted by one clock period, where the clock (CLK) operates at 250 MHz (i.e., period of 4 ns) and the reference sample pulse is generated by MOD-14 counter, which repeats for every 14 clock cycles.

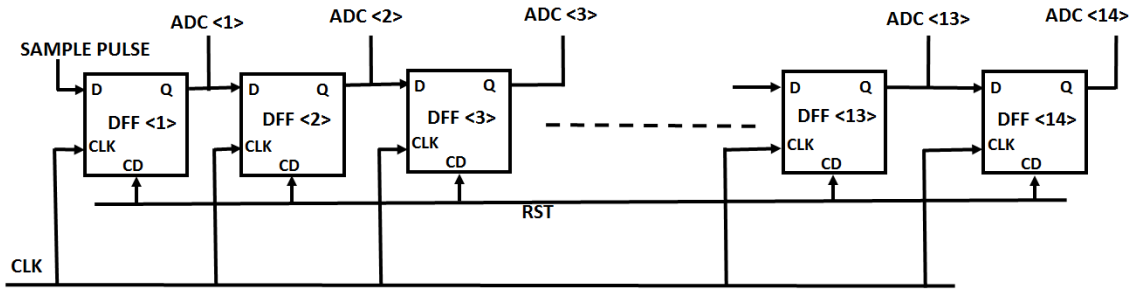

Figure 16. Block diagram of timing scheme

Fig. 17 shows the transient response of timing scheme for 14 time-interleaved SAR ADC, here the CLK operates at 250 MHz and reference sample pulse (SAMPLE PULSE) which repeats for every 14 clock cycles. The timing signals for operation of TI-SAR ADC (ADC< 1 > to ADC< 14 >) are shifted by one clock period without overlapping.

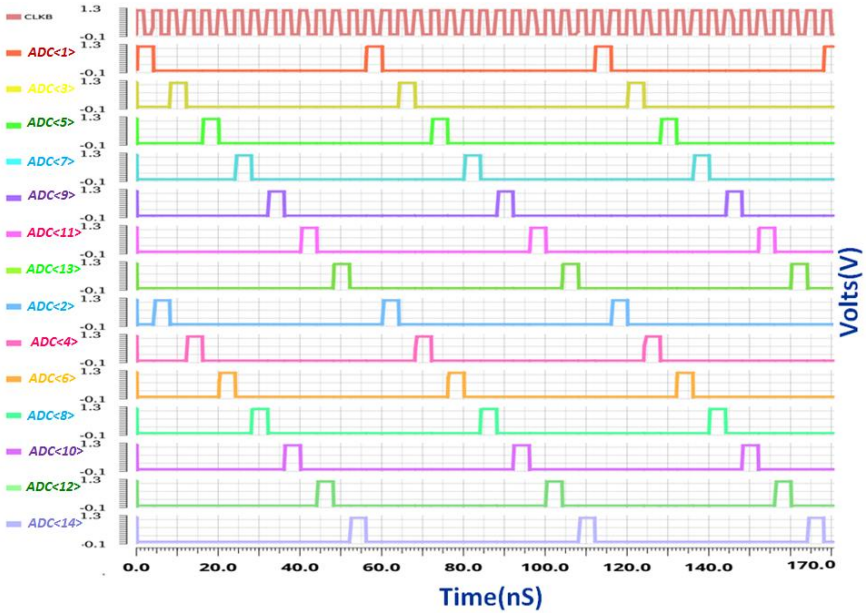

Figure 17. Transient response of timing scheme

5.3. Digital Multiplexing

Fig. 18 shows the block diagram of 14×1 digital multiplexing. In this design, the output data from each 10-bit SAR ADC (D < 1 : 10 >) is available at EOC. During rising edge of EOC the digital data from 14 TI-SAR ADC is latched into corresponding D-FFs (DFF1< 1 : 10 > to DFF14< 1 : 10 >). The latched data (D1< 1 : 10 > to D14< 1 : 10 >) is fed to corresponding 14 × 1 multiplexer and finally the multiplexed output data read in parallel combination, which is controlled by an MOD-14 counter (S < 1 : 4 >) operates at F_s = 250 MHz.

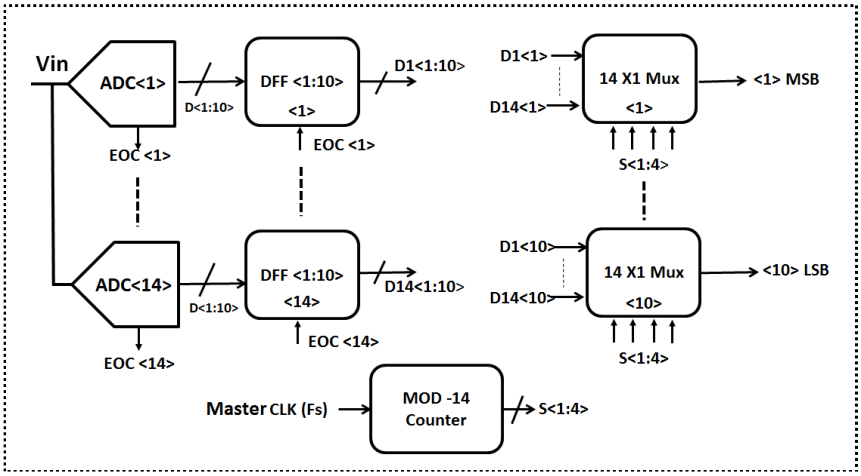

Figure 18. Block diagram of 14×1 digital multiplexing

6. SIMULATION RESULTS OF 14 TI-SAR ADC

6.1. Dynamic performance

The ideal 10-bit DAC is used to reconstruct sampled analog output voltages from the 10-bit digital outputs (D< 9 : 0 >) as shown in Fig. 19a, here D< 9 > represents the sign bit. The coherent sampling method is used for evaluating dynamic performance of TI-SAR ADC as shown in Fig. 19b. The transient noise simulation is carried out to include quantization, thermal noise effects (F_{max} is chosen as maximum clock frequency given for ADC i.e., 250 MHz). The following inputs are given for evaluating the dynamic performance of 10-bit TI-SAR ADC. V_{in} = 1 V_{p-p}, F_{in} = F_s/8 (33.6 MHz), F_s =250 MS/s and no. of sample points (N) is 128. The achieved SFDR is 66 dB and SNDR of 59.3 dB (ENOB = 9.6 bits). This results in a FoM value of 60 fJ/step.

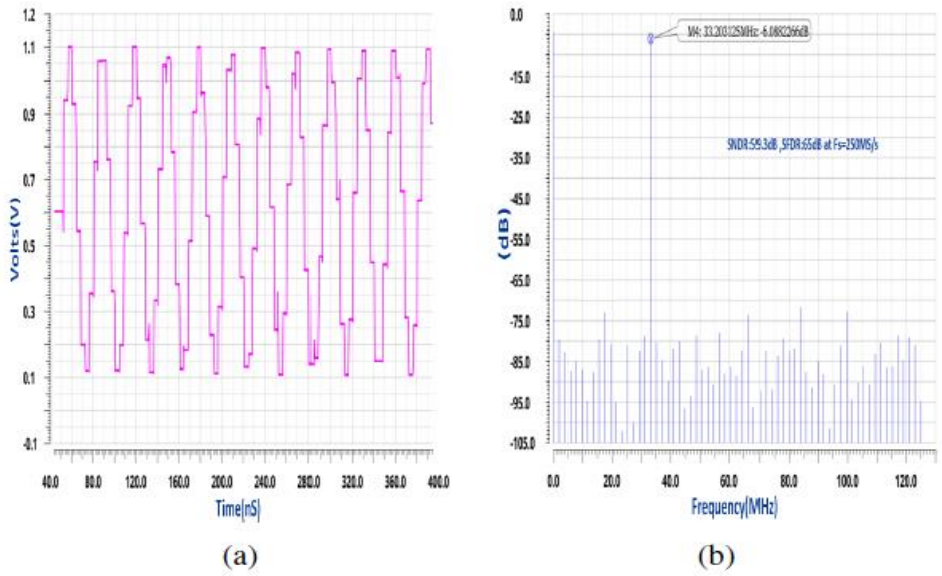

Figure 19. Single channel TI-SAR ADC (a) Transient response (b) Output Spectrum

7. PERFORMANCE SUMMARY AND COMPARISON

Table 1. Performance Summary of 10-bit SAR ADC

Parameter	**Value**
Process/Technology	UMC 65 nm CMOS Technology
Supply Voltage	1.2 V
Input Swing (differential)	2 V_{p-p}
Sampling Rate	15MS/s
Input Offset Voltage	±872 µV
SFDR	64.5 dB
SNDR	57 dB
ENOB	9.2 bits
Power consumption	560 µW
FoM	63.5 fJ/Step

Table 2. Comparison Table

	This Work	**ISSCC** [19]	**ISSCC** [20]	**VLSI** [21]	**JSSC** [22]
Architecture	SAR	SAR	SAR	SAR	SAR
Technology (nm)	65	90	65	90	65
Supply Voltage (V)	1.2	1	1	1	1.2
Sampling Rate (MS/s)	15	50	50	30	50
Resolution (bit)	10	9	10	10	10
Power (µW)	**560**	700	820	980	826
SFDR (dB)	64.5	-	-	68.16	61.8
ENOB (bits)	**9.2**	7.8	9.16	9.16	9.18
FoM (J/step)	63.5f	65f	30f	57f	27f

8. CONCLUSION AND FUTURE WORK

This paper describes about various architectures of time-interleaved ADCs, selection of number channels based on sampling rate and sub-ADC architecture. The mathematical model for 14 time-interleaved ADC has been developed to analyse the effect of gain, offset and timing mismatch among the channels. The design of 10-bit, 20 MS/s SAR ADC has been implemented in 65nm CMOS Technology. Layout design of 10-bit capacitive DAC, preamplifier based dynamic latch comparator is implemented by using common centroid method and their extracted views are included in simulations. The target sampling rate was 20 MS/s in this design, however the sampling rate achieved is 15 MS/s. As a result, the 10-bit SAR ADC operate at 15 MS/s with power consumption of 560 µW at 1.2 V supply and achieves SNDR of 57 dB (i.e. ENOB 9.2 bits) near Nyquist rate input. The design of 10-bit, 14 time-interleaved (single channel) SAR ADC has been implemented. The achieved SNDR of 59.3 dB (ENOB = 9.6 bits) and SFDR of 66 dB with power consumption of 11.6 mW. This results in a FoM value of 60 fJ/step.

8.1. Future Work

The future work following this are –

- Implementation of proposed 4-channel, 1 GS/s time-interleaved SAR ADC.
- Implementation of calibration techniques to overcome the non-ideal effects in time-interleaving ADC (offset, gain and timing mismatches among the channels).

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