A NEW SYSTEM ON CHIP RECONFIGURABLE GATEWAY ARCHITECTURE FOR VOICE OVER INTERNET TELEPHONY

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ABSTRACT

The aim of this paper is to present a new System on Chip (SoC) reconfigurable gateway architecture for Voice over Internet Telephony (VOIP). Our motivation behind this work is justified by the following arguments: most of VOIP solutions proposed in the market are based on the use of a general purpose processor and a DSP circuit. In these solutions, the use of the serial multiply accumulate circuit is very limiting for the signal processing. Also, in embedded VOIP based DSP applications, the DSP works without MMU (memory management unit). This is a serious limitation because VOIP solutions are multi-task based. In order to overcome these problems, we propose a new VOIP gateway architecture built around the OpenRisc-1200-V3 processor. This last one integrates a DSP circuit as well as a MMU. The hardware architecture is mapped into the VIRTEX-5 FPGA device. We propose a design methodology based on the design for reuse and design with reuse concepts. We demonstrate that the proposed SoC architecture is reconfigurable, scalable and the final RTL code can be reused for any FPGA or ASIC technology. Performances measures, in the VIRTEX-5 FPGA device family, show that the SOC-gateway architecture occupies 52% of the FPGA in term of slice LUT, 42% of IOBs, 60% of bloc memory, 8% of integrated DSP, 16% of PLL and the total power is estimated at 4.3Watts.

KEYWORDS

Voice Over IP, Systems on Chip, FPGA, OpenRisc, Design reuse

1. INTRODUCTION

VOIP is an emerging technology that uses the IP network for voice services as an alternative to the public switched telecommunication network (PSTN). The advantages over traditional telephony include:

- Lower costs per call, especially for long distance calls
- Lower infrastructure cost compared to the PSTN.

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The main challenges in designing a VOIP application are the quality of service (QoS), the capacity of the gateways and scalability of the hardware. Factors affecting the QoS are line noise, echo, the voice coder used, the talker overlap and the Jitter factor. The capacity of the gateway is related to the number of lines that can be supported in an enterprise environment. Most important VOIP solutions proposed in the market [1-3] are based on the use of a general purpose processor and a DSP circuit. In these solutions, parts of the application run on software on the general purpose processor and the other part of the application runs on the dedicated DSP hardware to meet some performances requirements. In order to increase the processing capabilities of these platforms, FPGAs circuits have been proposed devices have emerged as an alternative solution to built VOIP hardware platforms. Contrarily to DSP and general purpose processors, FPGAs enable rapid, cost-effective product development cycles in an environment where target markets are constantly shifting and standards continuously evolving. Most of these offer processing capabilities, a programmable fabric, memory, peripheral devices, and connectivity to bring data into and out of the FPGA. In [4-6], a first version of the VOIP architecture was presented. In this paper, we propose a new SoC architecture for VoIP application. The originality of our approach is that the proposed architecture is built around the OPENRISC-V3 processor also we propose a design reuse methodology for the generation of the VOIP gateway architecture. The benefit of using such a methodology is flexibility; scalability, reuse, rapid SoC prototyping, and the entire core component are available at free cost. This can also reduces the whole VOIP cost.
Section 2, gives a general presentation of VOIP. Section 3 deals with the proposed design methodology. In Section 4, the SOC gateway hardware architecture is presented. In Section 5, the primary synthesis and implementation results are presented and finally a conclusion is given in section 6.

2. GENERAL PRESENTATION OF VOICE OVER IP (VOIP)

Voice over IP had its starts in February 1995 when a manufacturer started marketing software that enabled a conventional computer equipped with a sound card, microphone and loudspeaker to phone another PC via the internet. Initially, the voice quality achieved was unsatisfactory but the principle behind it drew a great attention of public, thus the first area of application for VoIP: PC-to-PC was established. Subsequent to this introduction a number of manufacturers concentrated on developing similar software and consequently raised the question of compatibility among different systems. In 1996, the International Telecommunication Union responded by developing the H.323 standard. Afterwards, the focus was the possibility of placing long distance calls using voice over IP known as toll bypass; however this required setting up a connection between the telephone network (PSTN) and the data network, a task performed by so called Gateways [7]. The result has been additional application for VoIP including: PC-to-phone, Phone-to-PC and, when two gateways are used, Phone- to - phone communication. This last option was the catalyst in the establishment of a new provider group named ITSP (Internet Telephone Service Provider) that permits telephony over IP within the provider network using prepaid cards. To date, VoIP refers to the ability to transfer data and voice and also video on the single network. Figure 1 illustrates the basic operating principle of VoIP.

The human voice initially generates an analog signal. This signal is converted into a bit stream by an Analog/Digital (A/D) converter and then submitted to a multiple compression process. The Voice frames are integrated into a voice packet. First RTP (Real time protocol) packet with a 12 address byte header is created. Then an 8-byte UDP packet with the source and destination address is added. Finally, a 20 byte IP header containing source and destination gateway IP address is added. The packet is sent through the internet where routers ands switches examine the destination address. When the destination receives the packet, the packet goes through the reverse process for playback. A minimal VoIP implementation requires two functionalities. First, it should be able to connect to other VoIP phones and, second, voice data should be carried by the

Internet. The first requirement is fulfilled by using signaling. The second one is achieved by using speech coding algorithms.

2.1 VOIP Signaling

Signaling enables individual network devices to communicate with one another. Both PSTN and VoIP networks rely on signaling to activate and coordinate the various components needed to complete a call. In a PSTN network, phones communicate with a time-division multiplexed (TDM) Class 5 switch or traditional digital private branch exchange (PBX) for call connection and call routing purposes. In a VoIP network, the VoIP components communicate with one another by exchanging IP datagram messages. The format of these messages may be dictated by any of several standard protocols. The most commonly used signaling protocols –Session Initiation Protocol (SIP), H.323 and Media Gateway Control Protocol (MGCP). In this paper interest is given to the SIP protocol [8].

2.1.1 Session Initiation Protocol (SIP)

SIP is a signalling protocol for initiating, managing and terminating sessions across packet networks. These sessions include Internet telephone calls, multimedia distribution, instant messaging, and multimedia conferences. SIP invitations are used to create session that allows participants to agree on a set of compatible media types. SIP makes use of elements called proxy servers to help route requests to the user's current location, authenticate and authorize users for services, implement provider call-routing policies, and provide features to users. SIP also provides a registration function that allows users to upload their current locations for use by proxy servers. SIP clients are referred to a SIP User Agents, and may make peer-to-peer calls, though usually they register and setup sessions via a SIP proxy. SIP can run on top of several different transport protocols though it most commonly uses UDP over Internet Protocol. Figure 2 shows the SIP session establishment.

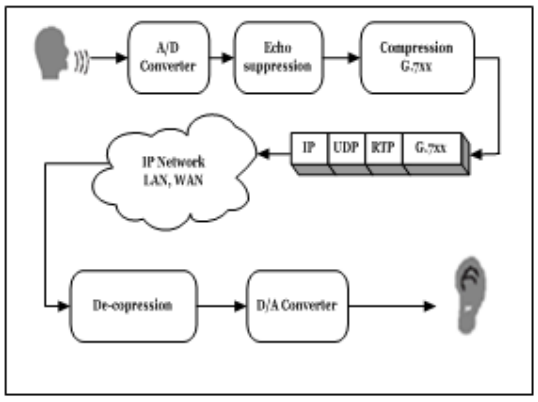

Figure 1. Principle of VoIP

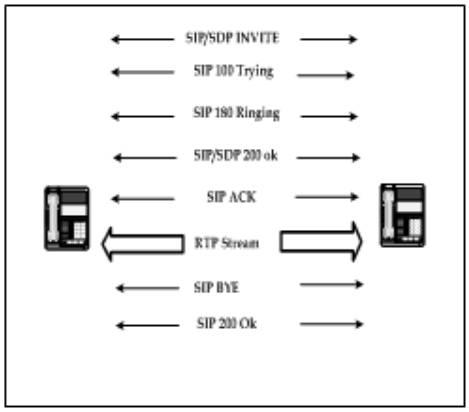

Figure 2. SIP Session Establishment

2.2 Speech coding Algorithms

The speech coding allows the reduction of transmission speech signal and communication channels to a limited bandwidth. The bandwidth of a transmission must be minimized while maintaining the quality of voice signal. Most codecs are algorithms, used to reduce the bit rate of speech data incredibly, while maintaining the voice quality. The most commonly used codecs in VOIP systems are: G.711 PCM [9], G.726 [10], ADPCM , G.729 LD-CELP [11], and G. 729/G.729a CS-ACELP [12]. PCM and ADPCM belong to the family of so called waveform

codecs. These codecs simply analyze the input signal without any knowledge of the source. Most of these codecs work in time domain, like PCM. These codecs offer high quality speech at a low computational complexity. But if we try to get the bit rate below 16 kbps the quality decreases tremendously.

Table1. Characteristics of the most coding algorithms

Coding algorithm		Bandwith (Kbps)	Algorithmic Delay (ms)	Complexity (MIPS)	MOS
G.711	**PCM**	64	0.125	0	4.3
G.726	**ADPCM**	16-40	0.125	6.5	2.0-4.3
G.728	**LD-CELP**	16	0.625	37.5	4.1
G7.29	**CSACELP**	8	10	17	3.4

To get the bit rate really down another approach is necessary. Source coders need to know the characteristics about the input being coded. Out of these characteristics a model of the source is made. When an input is encoded the source coder tries to extract the exact parameters of this model from the input. Then these parameters and a two state excitation is transmitted. These codecs can simply transport the pure informational content of a speech sample and not the voice itself. Their big advantage is that they operate with bit rates as low as 2.4 kbit/s. Hybrid codecs try to combine the advantages of waveform codecs, which is good quality, with the advantages of the source codecs that is low bit rate. To get the best excitation signal all possible waveforms are tested and the one with the least error is then chosen. This involves a very high computational complexity for every analysis frame. The low bit rate codecs usually involve a high computational complexity and a delay and the waveform codecs have the advantage of low delay and excellent quality. In Table 1 there is an overview of the quality of the different codecs according to the Mean Opinion Score. This score is derived from a large number of listeners who rated the quality of the played sample with a score from excellent (5) to bad (1). It should be understood that the various coding methods vary in the levels of complexity, delay characteristics and quality.

3. THE PROPOSED DESIGN METHODOLOGY

The proposed design reuse strategy is shown in Figure 3 as a process of Flow. In this figure, the methodology is based on a top-down design approach in which the user/designer is guided step by step in the design process of the VOIP gateway architecture. First, the user/designer is asked to choose the codec compression algorithm to be implemented and the number of lines that can be implemented. The compression algorithms that can be supported are the PCM G711 with a-law and μ-law, the G722 and G728 audio codec. The number of lines is related to the number of Ethernet that can be integrated. In the next step, a VERILOG code description of the SOC gateway architecture is generated. Before synthesis, functional simulation is required. Then, the VERILOG code is passed through a synthesis tool that performs Register transfer level (RTL) synthesis and optimization according to the target FPGA device family and under speed/area constraints. The result is a file ready for placement and routing. At this level, verification is also required before power analysis and then downloading the programming file into the FPGA prototyping board. To help the user/designer, documentation is available at each level of the design. It is to be mentioned that all the cores used in this design are downloaded from the OpenCores web site and are free of charge [13].

3.1 Design reuse

In our approach the design reuse methodology is exploited at two different levels. First, by using the cores of Opencores library, we exploit the Design with Reuse concept (DWR). Second, by creating a generic SOC gateway architecture, in which the cores can be modified, we can say that SOC-gateway is designed for Reuse (DFR).

3.2 Reconfigurability

The reprogrammabilty nature of the FPGA-Xilinx devices can be exploited to reconfigure the SOC Gateway architecture for different codecs' algorithms to achieve a better quality of service.

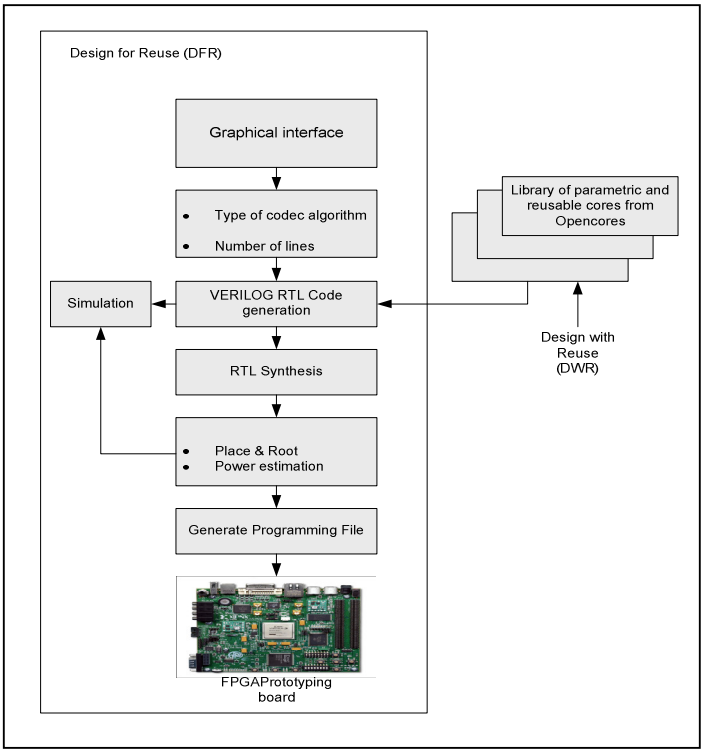

Figure 3 Proposed design methodology

4. THE PROPOSED SOC VOIP GATEWAY ARCHITECTURE

Figure 4 shows the proposed gateway architecture which is mainly based on the OpenRisc OR1200_V3 processor, a debug unit for debugging purpose, an Universal Asynchronous Receiver Transmitter (UART), an audio codec for voice compression, an AC97 audio controller, a standard MAC/Ethernet, a flash memory for internal boot, a DDR2 memory for embedded application and other interfaces for LCD display, keypad, Speaker and handsets. The cores are connected through the WISHBONE bus interface.

Figure 5 shows the OR1200-V3 internal architecture and Figure 6 shows the WISHBONE bus interconnection schema.

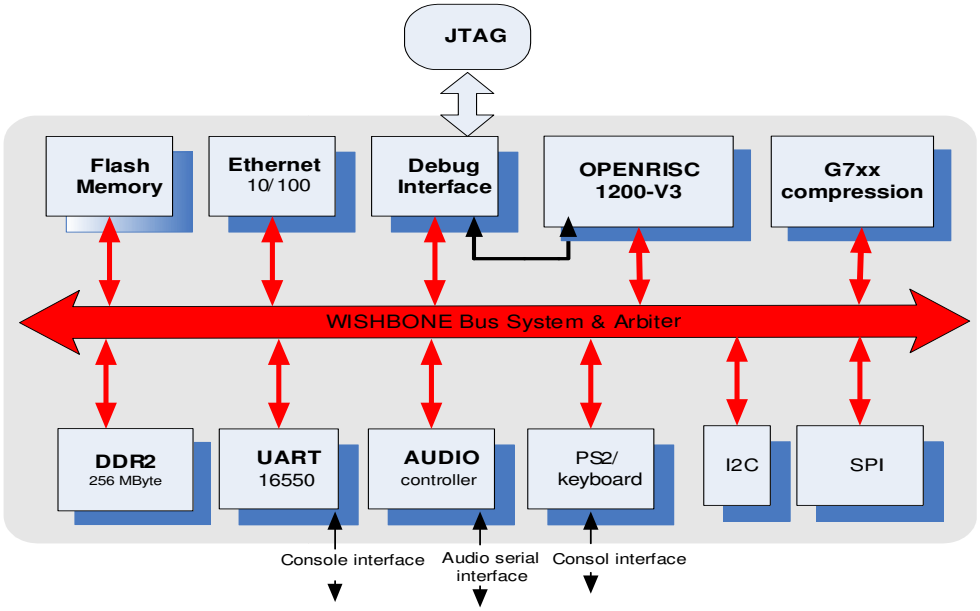

Figure 4 The VOIP Gateway general architecture

As shown in Figure 5, The OpenRisc 1200-V3 is a 32/64-bit RISC synthesizable processor with Harvard micro-architecture, 5 stage pipeline. It is developed and managed by a team of developers at OpenCores. An overview of the OpenRisc 1200-V3 architecture is illustrated in figure 5. The new features compared to the older version is that it support the new implementation of IEEE 754 compliant single precision FPU, also new instruction/data register MMU is added for embedded Linux distribution.

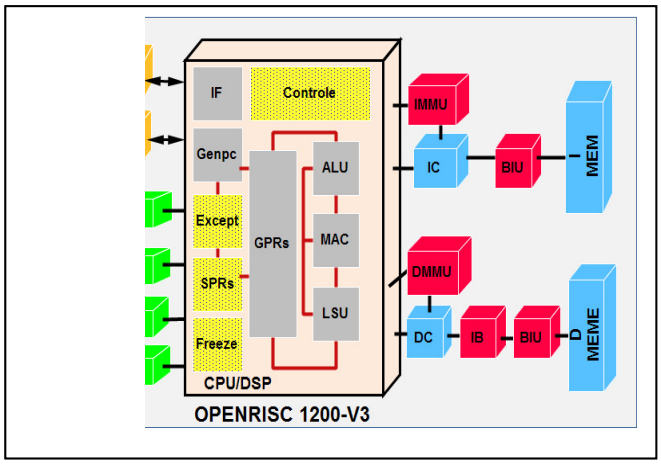

Figure 5. OR1200 Architecture

The WISHBONE bus interface uses a MASTER/SLAVE architecture. Some signals are specific to the master core, others to the slave one and there are common signals shared between the master and the slave. The MASTER interface could be on a microprocessor IP core, and the SLAVE interface could be on a serial I/O port (Figure 6).

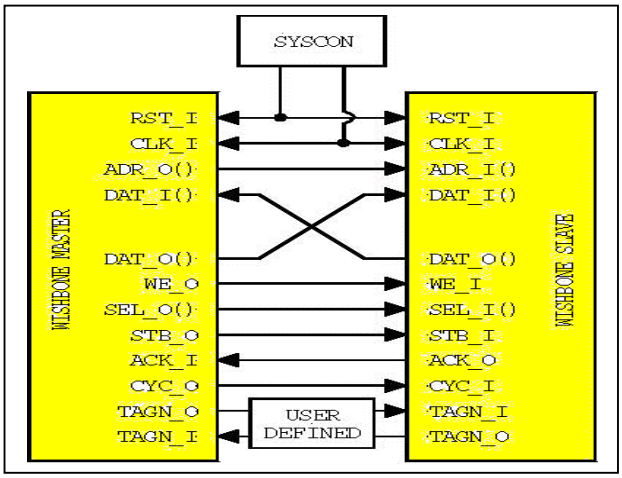

Figure 6. WISHBONE interconnect schema

In this architecture the WISHBONE uses the shared bus interconnection schema, thus a MASTER initiates a bus cycle to a target SLAVE. The target SLAVE then participates in one or more bus cycles with the MASTER. An arbiter determines when a MASTER may gain access to the shared bus. The main advantage to this technique is that shared interconnection systems are relatively compact. Generally, it requires fewer logic gates and routing resources than other configurations such as the cross bar switch configuration. Figure 7, shows the configuration of the wishbone bus which supports up to 8 masters and 16 slaves as well as 4 priority level. This characteristic can be explored to add more Ethernets and codec cores to boost the capacity and scalability of the gateway.

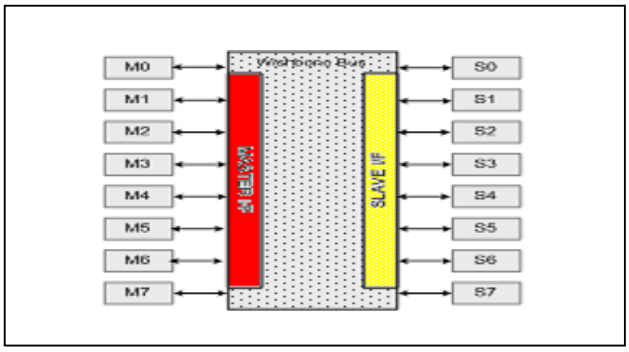

Figure 7. Whishbone core configuration

5. SYNTHESIS AND IMPLEMENTATION RESULTS

Our first implementation is a SOC that integrates the G711 algorithm, one MAC/Ethernet, the Openrisc-V3 processor, a debug unit, the UART circuit, the AC97 audio controller, a flash memory, a DDR2, I2C, SPI and PS2 keyboard.de. We performed synthesis and physical implementation using the Xilinx ISE design tool [14]. The whole architecture is mapped into the Xilinx FPGA VIRTEX 5 ML501 FPGA. Table 2 shows the synthesis results. Mainly, the SOC occupies 52% of the FPGA in term of slice LUT, 42% of IOBs, 60% of bloc memory, 8% of integrated DSP and 16% of PLLs. Table 3 shows the power dissipation in each FPGA module. Mainly, the total estimated power is 4.3 Watt. It is to be mentioned that IOs blocs and leakage

currents constitute the major source of power consumption. Another source of power consumption is the PLL module. In the other hand the DSP module consumption is zero. This is because the DSP integrates only few logics and is not really well exploited in this architecture. Figure 8 shows the final FPGA layout. It is clear that for other algorithm configuration or if more Ethernet cores are integrated, a migration to another FPGA device with more resources is necessary.

Table 2 Synthesis results

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	15098	28800	52%
Number of bonded IOBs	185	440	42%
Number of Block RAM/FIFO	29	48	60%
Number of DCM_ADVs	1	12	8%
Number of DSP48Es	4	48	8%
Number of PLL_ADVs	1	6	16%

Table 3 Power estimation

On Chip	Power
Clocks	0.291
Logic	0.006
Signals	0.011
BRAMs	0.015
DSPs	0.000
PLL	0.112
DCMs	0.094
IOs	3.209
Leakage	0.590
Total	4.328

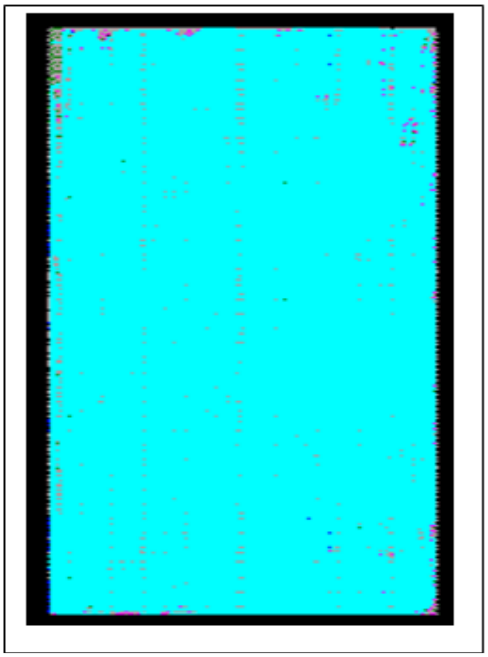

Figure 8 Final FPGA layout

6. CONCLUSION

We have successfully implemented into FPGA, a new SOC gateway architecture for VOIP application. By adopting a design reuse methodology, we demonstrated that the architecture is reconfigurable and scalable. Key features of this architecture are: the integration of different kind of compression algorithms and the possibility to add or remove the number of lines which related

to the MAC/Ehernet circuit. This work is still under progress. As future work, we aim first to optimize the architecture to achieve less power dissipation and less area resources of the FPGA. Then, we project to embed the RTP en UDP signaling protocols into FPGA to build an embedded VOIP server.

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