A 5.99 GHZ INDUCTOR-LESS CURRENT CONTROLLED OSCILLATOR FOR HIGH SPEED COMMUNICATIONS

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ABSTRACT

This paper presents the design of five-stage current controlled inductor-less ring oscillator that were simulated in Silterra 0.18um CMOS Technology with oscillation frequencies up to 5.99 GHz. The design uses cross coupled MOS devices along with active inductor (thus inductor-less) and controlled by current source to aid in switching speed and to improve the noise parameters. The simulations show that the five-stage oscillator achieves frequency in the range of 3.78GHz to 5.99GHz. The simulated phase noise of the same design was -115.67 dBc/Hz at 1MHz offset with a center frequency of 5.99GHz.

KEYWORDS

VLSI &CMOS, LC Oscillators, Phase Noise, Current Source, Active Inductor

1. INTRODUCTION

The Phase-locked Loop (PLL) is a critical component in many high-speed systems since it provides the timing basis for functions such as clock control, data recovery, and synchronization. The voltage/current controlled oscillators (VCO/CCO) is perhaps the most crucial element of the PLL because it directly provides output clock of the PLL.

Any CMOS oscillators can be built using ring structures, relaxation circuits, or an LC resonant circuit. The LC design has the best noise and frequency performance due to the large Q factor of the resonant networks [1]. However, LC circuit in CMOS process increases the cost and the complexity of the chip and also often time creates problems in controlling the eddy current.
On the other hand, oscillators with ring structure are easily built on any CMOS process and it is less complex and costly. The design is also very straight forward and it is also capable of providing multiphase outputs and a wide tuning range. Fig. 1 shows the conventional five-stage ring oscillator. The downside of this ring oscillator is compromised noise performance due to the missing passive LC network. In this article, we present a design that improves the overall characteristics of CMOS ring oscillators to be comparable to those of LC designs by replacing the passive LC network with the active version. The design also adds a current source instead of voltage source to increase the switching speed.

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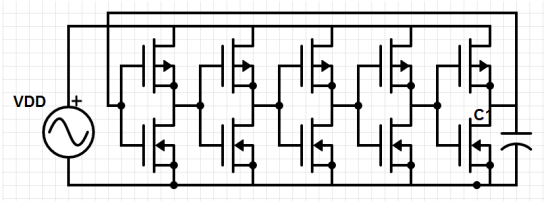

Fig. 1Conventional Five-Stage Ring Oscillator

2. CROSS COUPLED DELAY CELL WITH ACTIVE INDUCTOR LOAD

Fig.2(A) below shows the typical cross coupled delay cell with passive inductor load. These passive inductors in this circuit are realized using an on-chip spiral layout which suffers from huge area consumption, small inductance and strong interaction with the substrate. There are many ways to synthesize an inductor. Self-biased active inductors are one of them. There were some initial researches proposed for MESFET [2] and later re-developed for CMOS [3, 4]. Fig. 2(B) shows one such proposal.

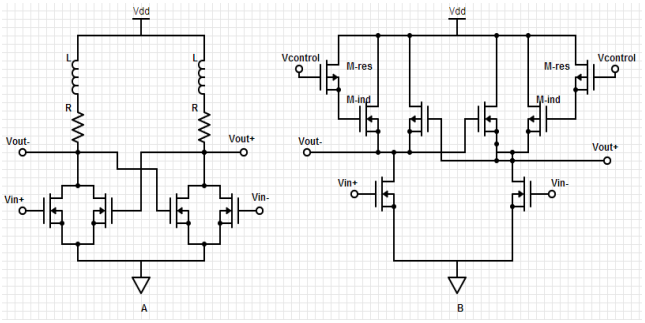

Fig. 2 VCO delay cell. (A) delay cell with passive inductor. (B) delay cell with active inductor.

M-res and M-ind forms the active LRC network. The circuits in Fig. 2(A-B) are simulated with square wave input and the output response isshown in Fig. 3. Note that the output of the delay cell with active inductor (B) is very similar to the one with the passive inductor (A).This is a huge achievement in replacing the passive inductor with the active inductor.

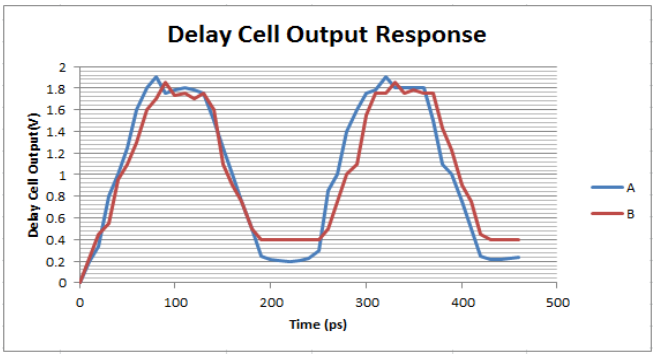

Fig. 3 Output voltage of VCO delay cell.
(A) Delaycell with passive inductor.
(B) Delay cell with activeinductor.

3. CURRENT MODE TECHNIQUE TO IMPROVE PHASE NOISE

The oscillation frequency of a CMOS inverter ring oscillator can be tuned either by adjusting its core supply voltage V_{DD} or its core supply current I_{DD} as shown in Fig. 4 below.

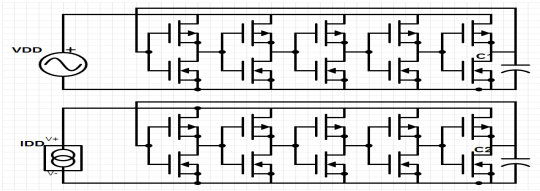

Fig. 4. Conventional Ring Oscillator with voltage modesupply (top)
and current mode supply (bottom).

Phase noise response for the five-stage conventional ring oscillator supplied with V_{DD} and I_{DD} are shown in the Table 1 below.

Table 1. Simulation results of Phase Noise at 1MHz offset
in Voltage Mode and Current Mode.

V_{DD} (V)	2.3	1.8	1.3
Phase Noise (dBc/Hz)	-88.7	-81.8	-79.1
I_{DD} (mA)	5.4	3.5	1.6
Phase Noise (dBc/Hz)	-92.3	-85.4	-82.7

It is clearly noted that the phase noise of the current controlled five-stage oscillator improves by about 4dBc/Hz as compared to voltage controlled. Silterra 0.18um CMOS technology was used in the design and simulation of the ring oscillator. To realize the current mode, PMOS current mirror technique implemented by using 3.3V I/O transistors. Fig. 5 depicts this.

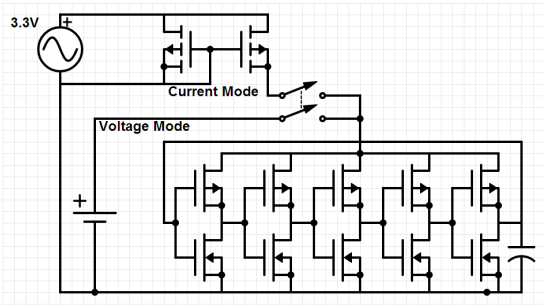

Fig. 5 Conventional ring oscillator implementing PMOS current mirror
and the connections for voltage mode and current mode supply.

4. PROPOSED INDUCTOR-LESS CURRENT CONTROLLED OSCILLATOR (ICCO)

Using the techniques described in Section 2 and Section 3 along with the negative delay skew techniques [5,6], a novel oscillator design has been proposed as shown in Fig. 6. Each stage of the

oscillator comprises of dual-delay cell with active inductor load scheme as depicted by Fig.2(B) and the PMOS current mirror for the current mode.

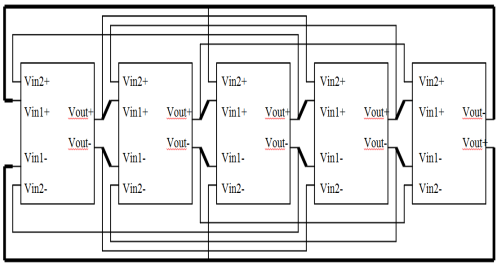

Fig. 6 Inductor-less Current Controlled Oscillator (ICCO)

The oscillator is laid out in Silterra 0.18um CMOS technology and later the parameters were extracted for simulation purposes. Fig. 7 shows the layout of the oscillator.

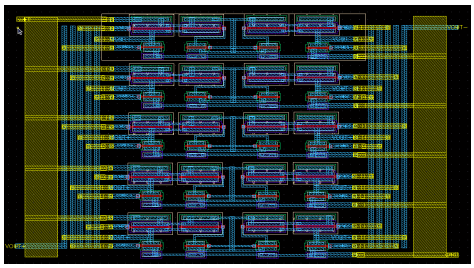

Fig. 7 Layout of Five-Stage ICCO.

The extracted device parameters were simulated using the same 0.18um process. The simulation reveals a peak oscillation frequency 5.99GHz and simulated phase noise of -115.67dBc/Hz at the oscillation frequency of 5.99GHz at 1MHz offset as shown below in Fig. 8. The driving capacitance for this oscillator has been set to 0.5pF for each stage and the supply for the current mirror has been set to 3.3V.

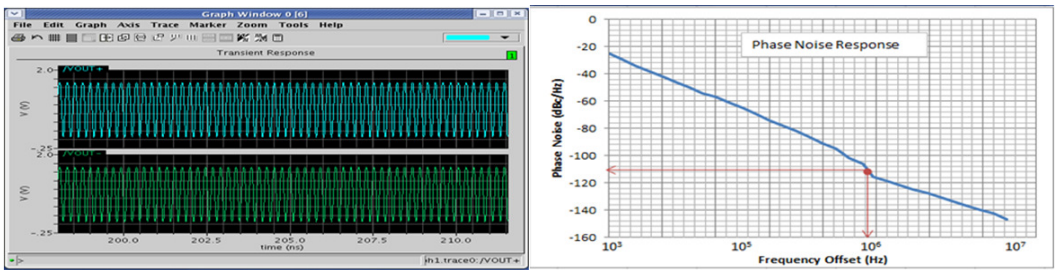

Fig. 8Simulated ICCO Oscillation of 5.99GHz and phase noise of -115.67dBc/Hz at 1 MHz offset.

Numerous simulations were carried out with various I_{DD} settings. Table 2(A-B) below shows the simulation setup and the simulated output frequency and the phase noise of the ICCO for various setting of the I_{DD}.It is quite apparent that I_{DD} needs to be above 2mA for decent phase noise performance. Thus only a current mode circuit can provide such a large current for comparable voltage mode MOS device configurations.

Table 2. (A) Simulation Setup . (B) Simulated Oscillation Frequency and Phase Noise (at 1MHz offset) of the ICCO for various I_{DD}

Simulation Setup	
Process	0.18um CMOS
Voltage	1.8v
Current Mirror Voltage	3.3v
Driving Capacitance	5pF per stage
Simulation Tool	Cadence's Spectre

(A)

I_{DD} (mA)	5.5	4.5	3.5	2.5	1.8
Osc Frequency (GHz)	5.99	5.45	5.16	4.97	3.78
Phase Noise (dBc/Hz)	-115.67	-113.45	-111.2	-107.89	-87.25

(B)

Table 3 below shows the comparison of this work against the other well-known works. It is clearly noted that this work excel in the oscillation frequency along with comparable phase noise. It is very interesting to note that the overall CMOS characteristics and process has improved dramatically when compared to the reported works especially [11] since it achieves almost same output frequency as this work. However, this work is much smaller in layout size (hence cheaper) since it is using active inductor as compared to passive inductor by [11] thus proving characteristics of CMOS has been improved through the replacement of passive inductor with active inductor.

Table 3. Comparison of this work against others

Ref	Technology (um)	Vdd (V)	Phase Noise (dBc/Hz)	Freq (GHz)
[7]	0.18 CMOS	1.8	-118.00	3.0
[8]	0.18 CMOS	1.8	-110.00	1.6
[9]	0.18 CMOS	1.8	-122.90	1.6
[10]	0.18 CMOS	1.8	-109.40	1.5
[11]	0.18 CMOS	1.8	-101.67	6.01
This Work	**0.18 CMOS**	**1.8**	**-115.67**	**5.99**

5. CONCLUSIONS

This paper proposes a current controlled oscillator for an improved frequency oscillation and with active inductor load for an improved phase noise. Achieving a phase noise of -115.67 dBc/Hz at 1MHz frequency offset and a peak oscillation at 5.99GHz is quite obvious that this is capable of being used in high speed communications applications.

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