HIGH SPEED LOW POWER CMOS DOMINO OR GATE DESIGN IN 16NM TECHNOLOGY

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ABSTRACT

Dynamic logic circuits provide more compact designs with faster switching speeds and low power consumption compared with the other CMOS design styles. This paper proposes a wide fan-in circuit with increased switching speed and noise immunity. Speed is achieved by quickly removing the charge on the dynamic node during evaluation phase, compared to the other circuits. The design also offers very less Power Delay Product (PDP). The design is exercised for 20% variation in supply voltage.

KEYWORDS

Low PDP design, High speed OR gate, Domino OR gate, Low power design.

1. INTRODUCTION

The rapid advancements in the field of VLSI is due to the increased use of battery operated devices such as laptops, PDAs, mobiles etc., advancements in wireless communications and computations are the urge for low power budgets and compactness. To achieve this, the transistor size has been continually scaled down and to have proper operation of the device, the supply voltages have also been scaled. As the technology aggressively scales down, the density on the chip has increased and hence the interconnection density, which increased the coupling capacitance of the circuit. This lead to increased interaction between the connections and thereby increasing crosstalk and system failures. On the other hand with the decrease in the supply, the gate threshold is decreased to preserve system throughput and so leakage currents have increased.

Dynamic logic circuits found their wide application in high speed, low power areas such as microprocessors, digital signal processing, dynamic memories etc., because of their low device count, high speed, short circuit power free and glitch free operation [2]. On the other hand it is also possible to design a dynamic logic unit that is smaller than its static counterpart. Dynamic logic consists of pull down network realizing the logic. From the basic theory of dynamic logic the circuit is pre-charged and evaluated at every clock cycle. When a dynamic gate is cascaded by a static inverter, it is called Domino logic. Due to high clock frequency, a large amount of noise

David C. Wyld et al. (Eds) : ACITY, DPPR, VLSI, WiMNET, AIAA, CNDC - 2015
pp. 135–141, 2015. © CS & IT-CSCP 2015 DOI : 10.5121/csit.2015.51312

gets induced and power consumption increases. The main draw backs in dynamic logic are charge sharing and cascading. To overcome these problems domino logic is used. Domino gates runs faster than the static gates as they present much lower input capacitance for the same output current and a lower switching threshold. In this paper we are proposing a technique to reduce the power and increase the speed of domino gate.

1.1 PROBLEM STATEMENT:

The basic domino logic stage consists of logic realized using N-MOS (Mn) in pull down network and the pull up net work consists of a single P-MOS (Mp) to pre charge the dynamic node to logic high as shown in Fig.1. The dynamic node is cascaded into a static inverter from where the gate output is taken and can be connected to the N-FET input of the next stage[1]. When clock =0, the dynamic node charges to V_{dd} and the bottom transistor Mn is responsible for holding the charge on the dynamic node irrespective of the input combination applied to the pull down network. Thus the output goes to logic 0 during this interval (pre- charge phase). When the clock = 1(evaluation phase) the pre-charge transistor (Mp) goes off, allowing the dynamic node to settle down to a state determined by the inputs . Based on the logic implemented, the charge on the dynamic node may be retained at logic 1, thus output remains at logic 0 or the dynamic node may get discharged to logic 0 and output may rise to logic 1.

During evaluation phase when all the inputs are at logic 0, dynamic node should be at logic 1, but the wide fan-in N-MOS leaks the charge stored on the dynamic node due to sub threshold leakage. This is again compensated by P-MOS keeper (Fig.2), which aims to restore the charge on the dynamic node. But when a noise pulse occurs at any of the input such that pull down network provides a direct path to ground, the keeper may not be able to retain the charge on the dynamic node and the node gets wrongly discharged. As the noise in Domino gates is becoming more important than area, power and delay issues in the sub micro meter regime , recently several techniques have been proposed [6],[7] to reduce noise in domino circuits. All the techniques have aimed at reducing the noise effect, but have several drawbacks related to area, power and delay.

In section II existing domino techniques were discussed, section III discusses the proposed scheme, simulation and results compared with other existing schemes is presented in section IV and section V presents the conclusion.

2. BACK GROUND AND RELATED WORK

To compensate the leakage at dynamic node a weak transistor called keeper transistor is used. It prevents the charge loss and keeps the dynamic node at strong high when pull down network is off. In the first Domino proposal [3] the gate of the keeper is connected to ground which makes it always ON. Thus at the beginning of the evaluation phase if the pull down network turns ON, the dynamic node tends to discharge through PDN and keeper starts injecting the lost charge to the dynamic node as it is always ON, which results in contention. This technique introduced a potential DC power consumption. In order to reduce this extra power dissipation, a feedback keeper was proposed in [4],[5]. In this the PMOS gate of the keeper (Fig.2) is connected to the output of the static inverter. Thus during Pre-charge the dynamic node is at high, and the keeper remains on and during evaluate phase if the pull down net work is on, dynamic node gets

discharged and the output node is at logic high which makes the keeper transistor off, thus eliminating contention.

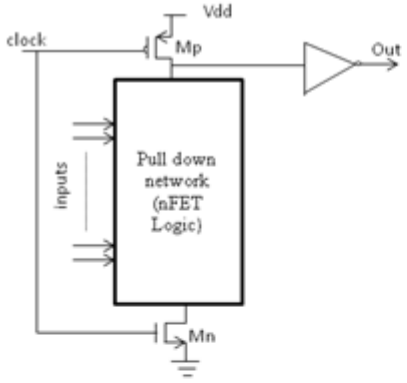


Fig.1 Basic Domino logic stage

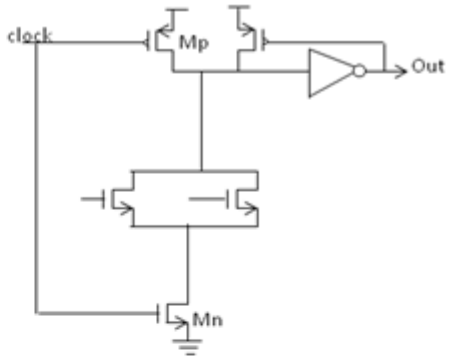


Fig.2 Standard Domino OR gate

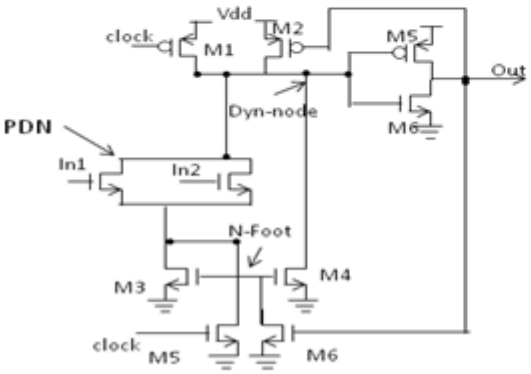


Fig .3 Diode Footed Domino[6]

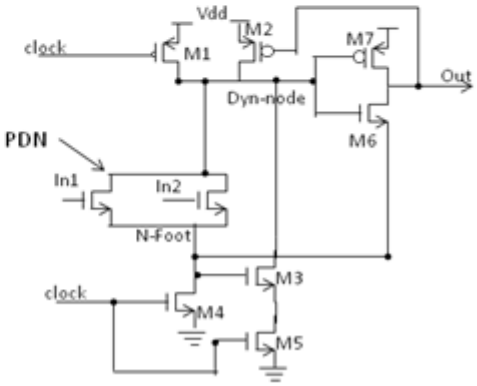


Fig.4 Domino circuit in Scheme [8]

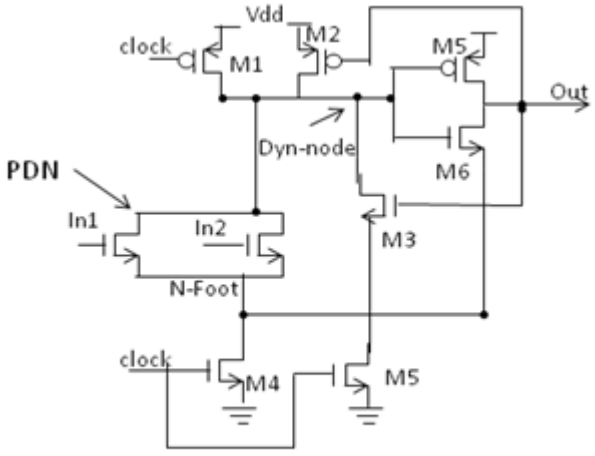


Fig.5 Proposed Domino circuit

In [6] a diode footed Domino was proposed (Fig.3), where an NMOS transistor Mn is connected in diode configuration. In this configuration, the leakage current flowing through the PDN in evaluation phase causes the drop across the diode transistor making Vgs negative, thus reducing leakage current. The performance degradation can be compensated by the mirror network. The inverted clock increases the capacitive load of the clock driver.

In [7] the circuit is based on pull-up network, consisting of only n-MOS transistors. This style does not have a p-MOS transistor. When the clock is low the pre-charge transistor M1 is switched on and the dynamic node is charged to 0v. When the clock is high, M1 is off and the dynamic node gets conditionally charged by the pull-up network to Vdd, but due to the absence of pull-up transistor, the node gets charged to Vdd-Vth and this drop is compensated by M2 the keeper transistor. This circuit needs an inverted clock which increases the capacitive load and area to invert the clock.

In [8] an additional evaluation transistor M5 is added in order to stack M3 and make its gate- to source voltage small, thus making the circuit noise robust and less leakage power consuming (Fig. 4). The performance degradation is compensated by widening the keeper transistor M2.

3. PROPOSED SCHEME

The proposed domino circuit is as shown in the figure 5. Transistor M3 and M5 are connected between the dynamic- node and ground and the gate ofM3 transistor is connected to the OUT terminal and M3 is stacked with M5. During evaluation phase when PDN is on with one or more inputs connected to logic one, the transistor M4 discharges the dynamic-node and the Out terminal goes to logic ‘1’ and M3 becomes on which aids in faster discharge of any accumulated charge on dyn_node along with PDN and M4. The rate of discharge can be controlled by changing the W/L ratio of M4. When all the inputs are at logic ‘0’, output stay at logic ‘0’ and M3 remains off and thus dyn_node retains its charge. If any input changes from logic ‘0’ to logic ‘1’ , PDN becomes conducting and during evaluation phase when clock is high, dyn_node discharges below the threshold voltage of the inverter turning its output to logic ‘1’. When output becomes logic ‘1’, M3 turns on providing a path to discharge dyn_node quickly as M5 is also ON during evaluation phase. At the same time as the source node of M6 being connected to N-foot, effect of noise in the circuit can also be reduced.

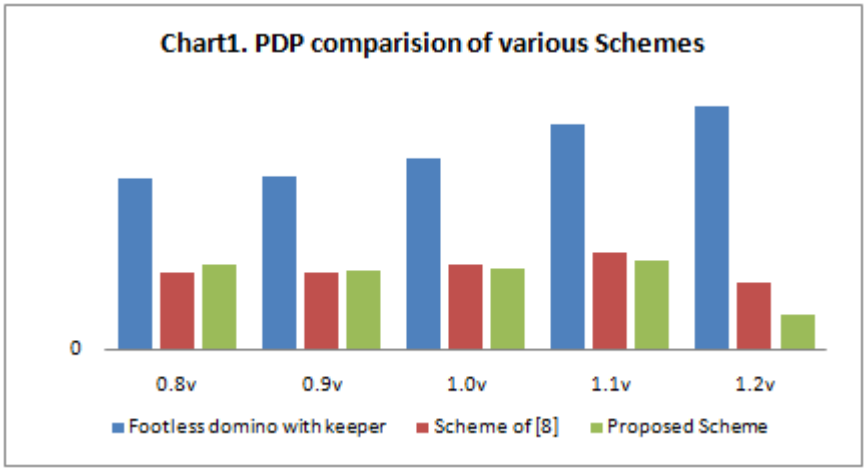
4. SIMULATION AND RESULTS

The circuits were simulated using Tanner T-spice using 16nm technology with 1V supply. The circuit was compared with OR gate of the existing techniques. The OR gate was implemented because it is a typical example of wide pull down network. It is found that the proposed circuit performs better than the previous circuits. The power and delay were measured using T-Spice and PDP was calculated. Delay for various circuits is measured using window technique. Table.1 shows the power and delay measured for basic domino with keeper, scheme proposed in [8] and the proposed circuit at different supply voltages. Table.2 and Chart 1 shows the PDP of the proposed circuit in comparison with the previous circuits. A plot of effect of supply voltage on delay is shown in Fig.6, and Fig.7 shows the simulated wave forms for a two input OR gate for various techniques. As can be seen from the wave forms the ripple in the Output is less in the proposed technique compared to the others thus reducing power dissipation. Output fall time is also less compared to other schemes, thus resulting in lower PDP

Table 1. Power and Delay comparison of the proposed scheme with existing schemes						
Supply voltage	Footless domino with keeper		Scheme of [8]		Proposed Scheme	
	Power	Delay	Power	Delay	Power	Delay
0.8v	2.55486E-06	1.4252E-09	7.49396E-07	2.15495E-09	1.40833E-06	1.26735E-09
0.9v	4.5318E-06	8.09909E-10	1.23397E-06	1.31192E-09	1.91414E-06	8.61012E-10
1.0v	6.79293E-06	6.00192E-10	1.74945E-06	1.02174E-09	2.40339E-06	7.18092E-10
1.1v	9.32268E-06	5.13905E-10	2.35983E-06	8.67323E-10	2.96814E-06	6.40169E-10
1.2v	1.18686E-05	4.34043E-10	3.16067E-06	4.44132E-10	3.48228E-06	2.10916E-10

Table 2. PDP comparison of the proposed scheme with existing schemes

Supply voltage	Footless domino with keeper	Scheme of [8]	Proposed Scheme
0.8v	3.64119E-15	1.61491E-15	1.78485E-15
0.9v	3.67035E-15	1.61887E-15	1.64809E-15
1.0v	4.07706E-15	1.78748E-15	1.72585E-15
1.1v	4.79097E-15	2.04673E-15	1.90011E-15
1.2v	5.15149E-15	1.40375E-15	7.34469E-16



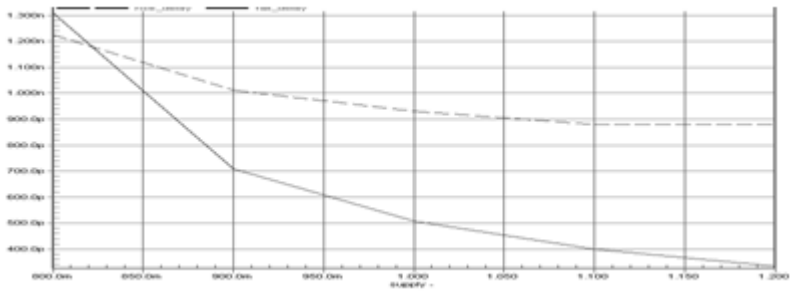


Fig. 6 Variation in Rise and Fall Delay for variation supply voltage

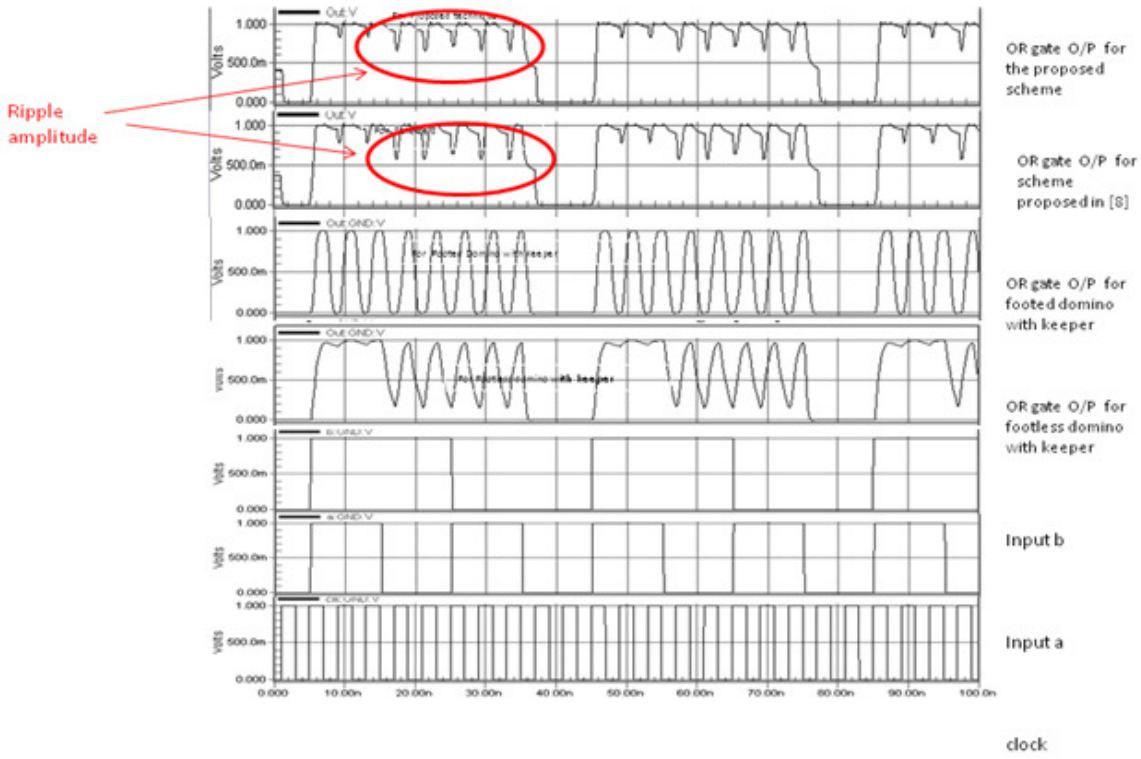


Fig.7 Simulation waveforms of Two input OR gate

5. CONCLUSION

In this paper we have proposed high speed low PDP domino logic circuit, which exhibits some noise tolerance at the output node. Simulations are done using Tanner T-Spice with PTM 16nm-low power technology files. From the results it is proved that the proposed design is better than the previous designs and offers about 29% reduction in delay and 3.5% reduction in PDP.

ACKNOWLEDMENTS

I would like to thank TEQIP-II for the facilities provided to carry out the work in the department.

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